state at approximately the inverse of the JFET threshold voltage. This voltage can be used to power the converter's control circuitry until the auxiliary winding is regulating. In Figure 1, a resistor and diode are used to connect the MOSFET voltage to the control circuity.

In order to successfully implement this startup, several conditions need to be met. The most critical item is what the under voltage lockout (UVLO) of the control circuitry is. Obviously, if the UVLO is set significantly higher than the JFET threshold, there will be a problem. In this design an UCC38C41 with a UVLO of 7.0 volts is used.

The next consideration is the impedance of the control circuitry when not powered, the JFET and MOSFET V_{DS} impedances with respect to the Input voltage, and their influence on the steady state MOSFET V_{DS}. This may seem complicated, but a straight forward method is to measure the cascode MOSFET V_{DS} vs. V_{in} with the Gate disabled and compare against the controller UVLO. If there is enough "head room" the approach is viable. R3 in the circuit can also be varied to influence the startup voltage.

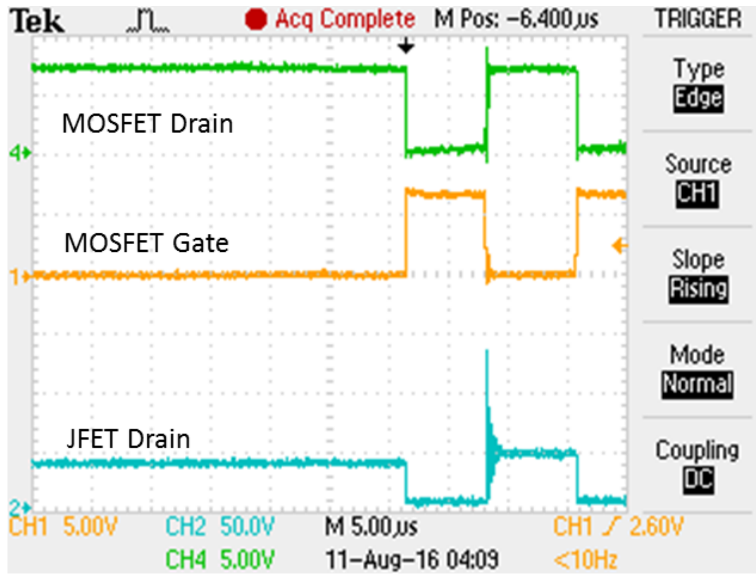

Figure 2: Cascode Startup Waveforms (R3 = 15 Ohms)

For verification, V_{in} is stepped to 200V, and Figure 2 catches when the supply begins to turn on, which is at 50 Volts.

4 Performance

Figure 3 is the efficiency of the converter at 35W and 55W across the entire input range(200 to 1000 Volts). The

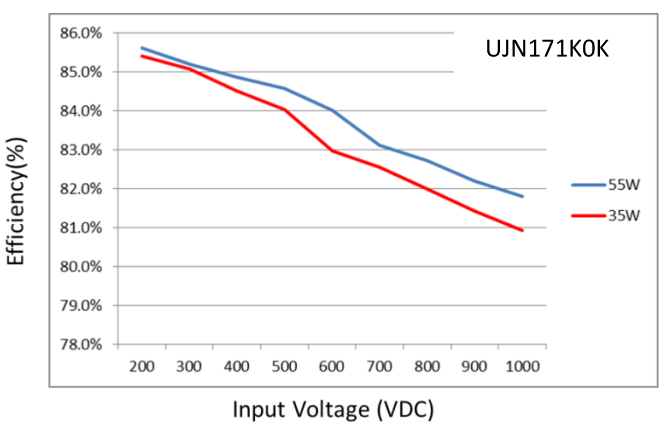

Figure 3: USCi Utility Power Supply
Efficiency vs. Output Power (V_{in}: 200V to 1000V)

power level is varied by changing the load on the higher current +12 Volt output, while the +5V output is fixed at 1.25 Watt and -12V output at 8 Watt. The switching frequency is 74 kHz. The efficiency for both power levels is greater than 85% at low line, while dropping in the 81% to 82% at high line.

5 Load and Line Regulation

The high current +12V output is regulated by a TL-431 using a CNY17F opto-coupler to maintain isolation between the primary and secondary side. Graphing the +12V output voltage from the data that generated the efficiency chart in Figure 3, the line regulation is measured at 0.09%, per given power level, and a 0.08% delta in output voltage variance between the two load values.

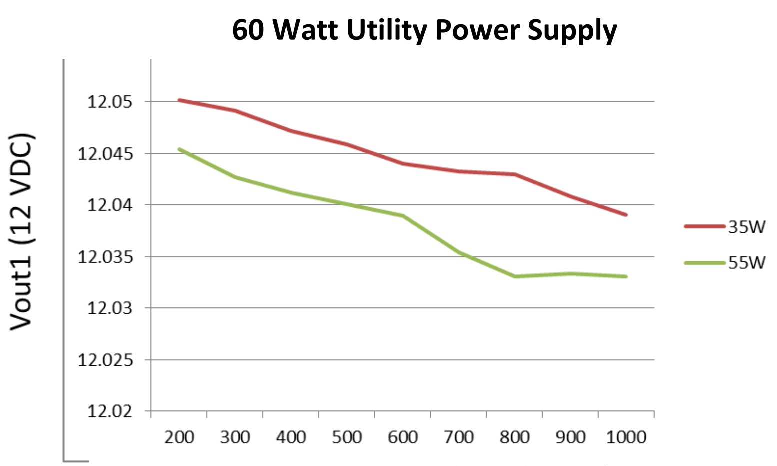

Figure 4: Line and Load Regulation

6 Output Ripple

In flyback supplies it is the designer decision on whether to use LC filters on the output. In this case, LC filters were not used in the initial design. The measured 200 mV pk to pk of output ripple on the Opto regulated +12 V output (3 Amp) is shown in Figure 5. As this equates to a ripple percent of 1.67%, and should be acceptable in most ripple requirements, LC filters were not added in subsequent board revisions.

7 Transformer

The flyback transformer (coupled inductor) in this design uses an EPCOS gapped pot core (B65813J160A87). The windings for the primary are 46 Turns of 25 AWG. The secondary's are +12V (4 Turns 18 AWG), -12V (4 Turns 22 AWG), +5V (2 Turns 22 AWG), and the +12V auxillary winding (3.5 Turns 22 AWG).

In order to minimize leakage inductance, the first 23 turns of the primarily are wound on to the bobbin, and then the secondary windings are added in a single layer across bobbin. The final 23 turns for the primary are then added.

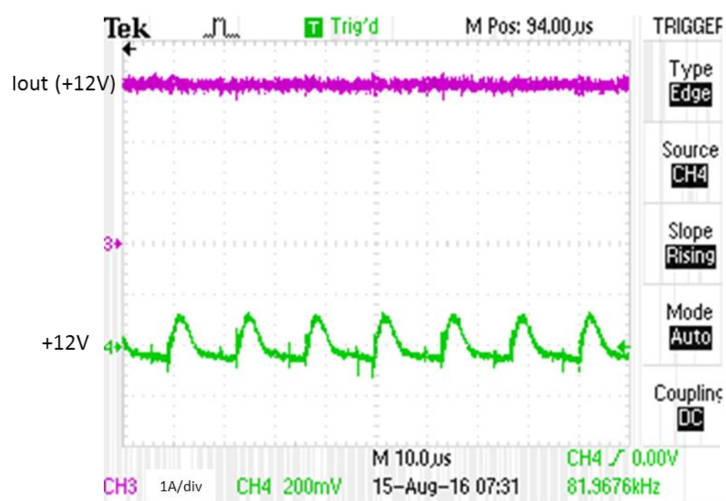

Figure 5: +12V Ripple 200mV pk to pk (Iout=3 Amps)

There are many approaches in implementing a magnetic design, so feel free to experiment.

8 Summary

This application serves to show that a JFET utilized in a cascode configuration can not only deliver high efficiency power conversion, but it also can simply the startup circuity, and thus reduce part count, board space and all the corresponding costs that are associated.

References

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