1200 V xJ SiC Series
45 mΩ,1200V - Normally-on JFET Transistors

Product Qualification Report

Summary

This report delineates the reliability and qualification tests applied to the 1200 V SiC normally-on JFET transistor product family from USCi packaged in 3 lead TO-247. USCi continuously strives for excellence by performing the harshest of reliability tests as outlined below in Table 1. A total of 924 devices were tested in 3 lots where the testing and failure criteria are based on *Stress Test Qualification for Automotive Grade Discrete Semiconductors* (AEC-Q101-REV-C) and the *Stress-Test-Driven Qualification of Integrated Circuits* (JESD471I). All reliability tests were performed in an ISO 9001 certified facility.

Table 1: USCi's Standard Reliability Qualification Tests
A: Tests Performed on 924 Units of 45 mΩ ,1200 V Devices

Test	Conditions	Sample Size	Reference Document
High Temperature Reverse Bias and Gate Bias (HTRB/GB)	T_{amb}=175ºC for 1000 Hrs, V=80% V_{max}	3 Lots of 231 devices (77pcs/Lot)	JESD22-A108C
Intermittent Operational Lifetime (IOL)	ΔTj ≥125ºC, 3000 cycles (5 minutes on/ 5 minutes off)	3 Lots of 231 devices (77pcs/Lot)	AECQ101C & MIL-STD-750D METHOD 1036,1037
Accelerated Moisture Resistance Unbiased Autoclave (AC)	T_{amb}=121ºC, 100% rh, 205 Kpa, 96 Hrs	3 Lots of 231 devices (77pcs/Lot)	JESD22-A102C
Temperature Cycling (TC)	-55ºC to +150ºC 2 cycles/Hr, 1000 cycles	3 Lots of 231 devices (77pcs/Lot)	JESD22-A104D, Cond H, Soak Mode 2

High Temperature Reverse Bias and Gate Bias (HTRB/GB)

The HTRB/GB test for normally-on JFET is designed to accelerate the failure modes within the active area as well as at the edge termination process under reverse bias by testing the device at steady state reverse voltage and increasing the ambient temperature. For normally-on JFET

transistors, a constant negative gate voltage is applied throughout the test to keep the JFET in its off-state. The device junction temperature is related to the ambient temperature and the leakage currents through:

$$T_j = (R_{th,case} + R_{th,heatsink})(I_{D,leak}V_{DS} + I_{G,leak}V_{SG}) + T_{Amb}$$

Intermittent Operational Lifetime (IOL)

Intermittent operational lifetime testing is aimed at accelerating failure modes associated with the stresses on all bonds and interfaces between the chip and mounting surfaces by subjecting the devices to repeated turn on and off of current. Self-heating within the device creates a junction temperature rise given by:

$$\Delta T_j = (R_{th,case} + R_{th,heatsink})I_D V_{DS}$$

Accelerated Moisture Resistance Unbiased Autoclave (AC)

Unbiased autoclave testing evaluates the moisture resistance integrity of non-hermetic packaged solid state devices using a moisture condensing environment under high pressure. The test accelerates moisture penetration through the external protective material (encapsulant or potting) or along the interface between the external protective material and the metal conductors passing through it.

Temperature Cycling (TC)

Temperature cycling is to evaluate the robustness of the whole package when undergoing extreme temperature swings while the devices are unbiased. Temperature cycling is used to identify failure modes associated from a mismatch in the coefficient of thermal expansion (CTE) between dissimilar materials of all the materials in the complete package.

Failure Criteria

Test failure criteria are defined by the AECQ101-REV C and JESD47I documents, summarized below as any device exhibiting the following:

1. Devices not meeting the electrical test limits defined in the device datasheet specification after performing each stress test.
2. Devices not remaining within ± 20% of the initial reading of each test after completion of environmental testing.
3. Any device exhibiting external physical damage attributable to the environmental test.

For any failure found, the root cause is found by implementing a Failure Mode Effect Analysis (FMEA) and is used to determine if the failure results from mishandling, ESD, test-equipment failure, or a data-acquisition failure. Any device failing for these reasons will be removed from the test and not counted as a qualification failure.

Summary of Reliability Qualification Results

Table 2 summarizes the failures and results for each test condition.

Table 2: Summary of Qualification Results
A: 924 Units of 50 mΩ, 1200 V Devices

Test	Conditions	Sample Size	Failed
High Temperature Reverse Bias and Gate Bias (HTRB/GB)	T_{amb}=175ºC for 1000 Hrs, V=80% V_{max}	3 Lots of 231 devices (77pcs/Lot)	0
Intermittent Operational Lifetime (IOL)	ΔTj ≥125ºC, 3000 cycles (5 minutes on/ 5 minutes off)	3 Lots of 231 devices (77pcs/Lot)	0
Accelerated Moisture Resistance Unbiased Autoclave (AC)	T_{amb}=121ºC, 100% rh, 205 Kpa, 96 Hrs	3 Lots of 231 devices (77pcs/Lot)	0
Temperature Cycling (TC)	-55ºC to +150ºC 2 cycles/Hr, 1000 cycles	3 Lots of 231 devices (77pcs/Lot)	0

USCi's xJ normally-on JFET transistor products were selected and stress tested in an ISO 9001 certified facility according to *JESD47I* and *AECQ101-Rev C* guidelines as outlined in this report. The devices tested met all electrical performance requirements, and no failures were observed in any of the qualification tests. Based on these results, USCi's xJ 45 mΩ,1200 V normally-on JFET transistor product is certified† as qualified product according to USCi's internal requirements.

† This report and its conclusions do not imply any guarantee, warranty, or suitability for any purpose regarding the products mentioned. Results represent the particular devices tested, which were randomly selected according to the sampling plan described herein.

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