1.5 kW Totem-pole PFC Using 650V USCi SiC Cascodes

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Totem-Pole PFC

1 Introduction

The large reverse recovery charge of conventional Si devices limits the totem-pole PFC to critical conduction mode (CrM) which suffers from large EMI noise and is suitable only for low power level. USCi 650 V SiC cascodes provide very fast switching speed, low on resistance, low reverse recovery charge (Qrr), low capacitance, standard 12 V gate drive and very good short circuit and avalanche capability. All these features make the SiC cascode ideal to enable a continuous conduction mode (CCM) totem-pole PFC. The excellent Qrr and fast switching performance of USCi 650 V SiC cascodes achieves 98.6% efficiency at high line (230 VAC) with 400 V DC output.

2 Totem-Pole PFC Topology

The goal of a totem-pole PFC is to reach and exceed the 80 PLUS Titanium efficiency standard. Generally, bridgeless PFC has lower conduction loss than conventional PFC by reducing the number of semiconductor devices in the current path from 3 to 2. Totem-pole bridgeless topology is known for its lower EMI noise with the least amount of devices when compared to other bridgeless topologies [1].

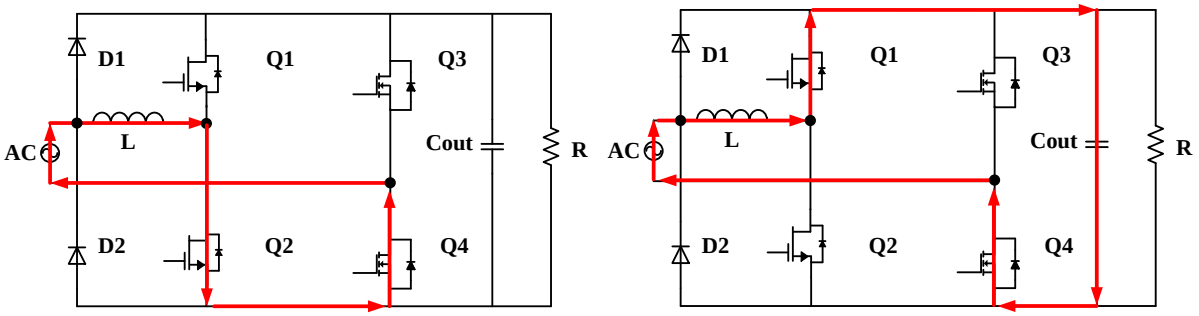

Figure 1. CCM totem-pole PFC operation in positive half cycle with an active switch in conduction (top) and a freewheeling device in conduction (bottom).

Fig. 1 illustrates the operation principle of a CCM totem-pole PFC during the positive half line cycle. Q1 and Q2 are the SiC cascodes to form the 100 kHz fast switching leg. Q3 and Q4 are low RDS(on) switches to form the line frequency slow switching leg. D1 and D2 are surge current diodes for soft start-up of the circuit. During the AC line positive half cycle, Q4 is always conducting the inductor current. The fast leg devices, Q2 and Q1, together with the input inductor and output capacitor form the simple boost converter topology. Q2 is the active switch and Q1 acts as the freewheeling boost diode. For the negative half cycle, Q3 is conducting the inductor current while Q2 and Q1 swap their functionality. To further boost efficiency, Q1, Q2, Q3, Q4 are all operating in synchronous conduction mode when possible.

3 Totem-Pole PFC Design Considerations

The input inductor is designed to keep the current ripple under 20% of the maximum peak input current, I_{in_pk}. The maximum peak input current occurs at low line and full load. Equation (1) gives the minimum inductance to operate in CCM at full load. D is the duty ratio of the active switch (Q1 or Q2) of the fast switching leg. Vout is the 400 V DC output voltage. Vin_min is the 115 Vac low line input voltage. Pout is the 1.5 kW rated output power. And fsw is the switching frequency of the fast leg. The minimum inductance value is therefore 271.1 µH. For fabrication simplicity, 300 µH is selected as the nominal design value for this boost inductor.

$$L \geq \frac{D(1-D)V_{out}V_{in\_min}}{0.2 * \sqrt{2}P_{out}f_{sw}} \quad (1)$$

For this prototype the inductor is fabricated with 2 stacks of C055438A2 MPP cores. The winding consists of 25 turns of 2-strand AWG-14 magnet wires. The inductance is 150 µH at full load and 350 µH at no load. The inductor DC resistance is 14 mΩ.

The output capacitance is determined based on two constraints, load hold-up time and output voltage ripple regulation. In this design, the hold-up time is set to be one AC line cycle and the output voltage peak to peak ripple is set to be 10 V.

$$C_{out} \geq \frac{2P_o t_{holdup}}{V_o^2 - V_{o\_min}^2};\ C_{out} \geq \frac{P_o}{2V_o \pi f_{line} V_{ripple}} \quad (2)$$

To meet both criteria, two 560 µF, 500 V aluminum electrolytic capacitors are used in parallel for this prototype.

The +12/-5 V gate drive is designed with isolated DCDC power supply module, RP-1212D, and -5 V linear voltage regulator, LT1175CS8-5#PBF. It is important to use isolated DCDC power supply module with very small isolation capacitance to reduce common mode noise from the switch node fast dv/dt transients.

The zero-crossing current spike is an inherent challenge of totem-pole PFC. This phenomenon will increase THD and decrease power factor. It is caused by the sudden discharge of the parasitic output capacitance of Q3 (from positive to negative cycle zero-crossing) or Q4 (from negative to positive cycle zero-crossing) when the corresponding fast leg active switch turns on. For example, during a zero-crossing from negative to positive cycle, Q2 becomes the active switch in the fast leg. Since input voltage is nearly zero, in order to output 400 V the duty ratio of Q2 is almost 100% while Q4 was blocking 400 V during the negative half cycle. Therefore, when Q2 turns on, the charge stored in the parasitic output capacitance of Q4 will incur a positive current spike on the input inductor. To gradually discharge the parasitic output capacitance of the slow leg Si MOSFET multiple gate pulses with small duty ratio are applied after a blanking window at zero-crossing. Experimental results show a very good mitigation of zero-crossing current spikes with this method.

4 Experiment Result

Figure 2 is the prototype of the 1.5 kW hard switched CCM totem-pole bridgeless PFC. No input filter is used for the measurement. Both AC input and DC output are floating. All voltage waveforms are obtained through differential probes. The input power, PF and THD is measured by a Tektronix PA1000 single phase power analyzer. The output power is measured by two Keysight 34465A digital multimeters.

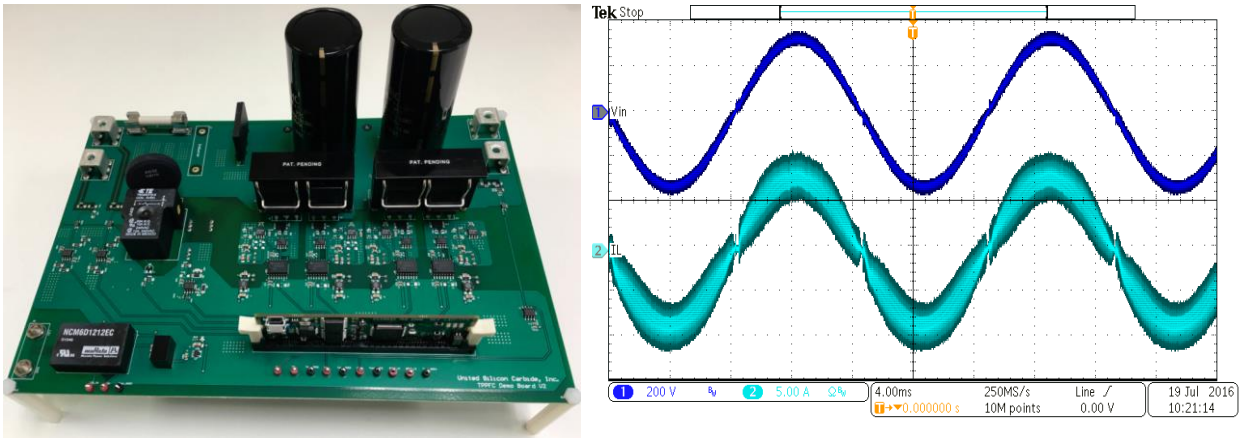

Figure 2. 1.5 kW hard switched CCM totem-pole PFC prototype (left) and input voltage, inductor current at 230 VAC, 1.3 kW load (right).

Figure 3 shows the efficiency curve measured at 230 VAC with 0 Ω turn-on gate resistor and 10 Ω turn-off gate resistor for the UJC06505K. 98.6% peak efficiency and 1.83% THD is achieved with 230 V AC input at 100 kHz switching frequency.

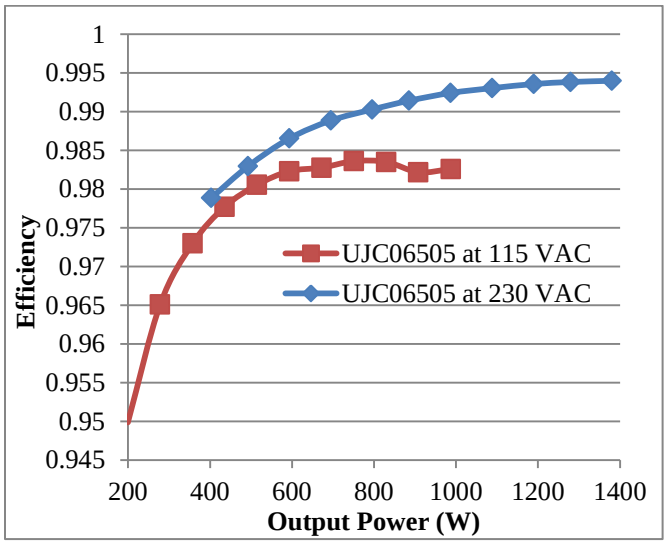

Figure 3. Efficiency and THD at 230 VAC input

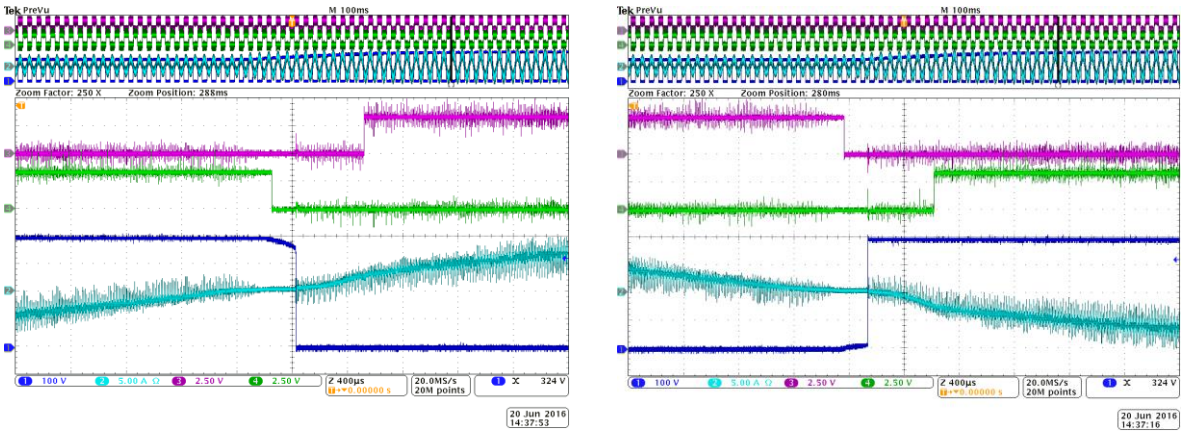

Figure 4. Inductor current (light blue CH2) at zero crossing, from negative to positive (left), from positive to negative (right). (CH1: VN potential to DC output ground; CH3: DSP gate signal of Q4; CH4: DSP gate signal of Q3)

As shown in Figure 4, with a blank window and low duty ratio gate pulses of the active device in the fast switching leg, current spikes near zero-crossing is greatly reduced.

5 Conclusion

A hard switched CCM totem-pole PFC is realized using the USCi UJC06505K 650 V SiC cascodes. With synchronous switching implemented to the full bridge, 98.6% peak efficiency is achieved at 100 kHz switching frequency in the fast switching leg with 230 V high line condition. The low RDS(on), low Qrr and fast switching capability make 650 V SiC cascodes ideal for full-bridge and half-bridge hard switching applications. Figure 2 demonstrates that the input inductor current follows the input AC voltage very well. Figure 4 illustrates that current spike near zero-crossing of input AC voltage is substantially alleviated by a blank window and multiple gate pulses of the active switch in the fast leg with small duty ratio.

References

[1] Q. Li, M. A. E. Andersen and O. C. Thomsen, "Conduction losses and common mode EMI analysis on bridgeless power factor correction," *2009 International Conference on Power Electronics and Drive Systems (PEDS)*, Taipei, 2009, pp. 1255-1260.