650V Cascode in LLC Second Stage Power Conversion for Servers

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Abstract

The 80 Plus certification program is used to classify power supplies in terms of efficiency and power factor. Supplies with the highest overall efficiency and power factor can be certified to the 80 Plus Titanium level. Titanium power supplies have the lowest energy cost, and are one of the pieces in improving operational computer efficiency.

There are two main power conversion stages that need to be optimized in order to meet a Titanium rating. The first is the power factor correction AC/DC stage, which is typically optimized with a "bridgeless" topology. The second is a DC/DC stage that is typically done with a soft switch topology such as a Phase Shift Full Bridge (PSFB) or an LLC. The LLC typically delivers the highest efficiency when optimized for a given operating point, as it has soft switching at both transitions, where the PSFB typically has higher efficiency over a wider operating range, but has soft switching on only one edge.

This application note highlights the LLC efficiency with respect to load and line variation. The converter in this application note uses a Texas Instruments UCC25600 controller, and it is recommended to read the datasheet and corresponding application notes for a more complete analysis. The simplified schematic is shown in the appendix.

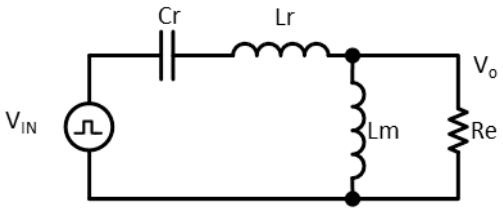

Figure 1: LLC equivalent circuit

1. Overview of an LLC Converter

The equivalent circuit of an LLC converter is shown in Figure 1. The V_{in} source is a square wave generated by a half bridge operating at 50% duty cycle, typically operating off a high voltage rail. The prime resonant frequency is set by L_r and C_r, which are discrete components, and L_m being the primary inductance of the transformer. The output load is reflected back to the primary and is represented by R_e.

$$Gain(f) = \frac{\frac{j\omega L_m R_e(V_{in})}{j\omega L_m + R_e(V_{in})}}{\frac{j\omega L_m R_e(V_{in})}{j\omega L_m + R_e(V_{in})} + \frac{1}{j\omega C_r} + j\omega L_r}$$

Equation 1 : LLC equivalent circuit Voltage gain

In the analysis, all waveforms are considered to be sinusoidal (first harmonic approximation). The gain ($V_o/(V_{in}/2)$) is shown in equation 1 (V_{in} is half due to the 50% duty cycle, and note that $\omega = 2\pi f$). The plot of that gain is shown in figure 2.

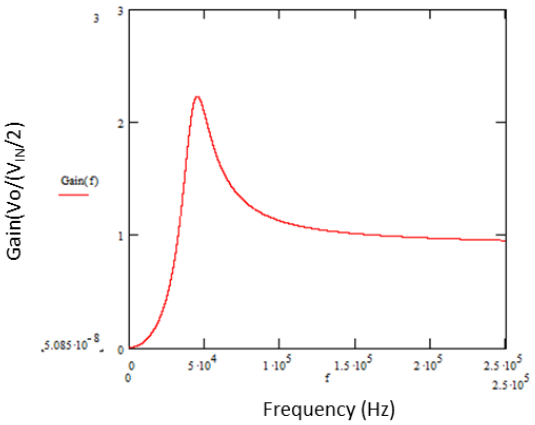

Figure 2: LLC gain plot

An LLC regulates by frequency modulation. By inspection, one can observe the gain peak and how that may complicate stability. It is therefore prudent to regulate on the right side of the peak where gain is less than ~1.2.

On the right side of the gain peak, from a regulation-frequency dynamic perspective, if the input voltage were to drop, or the load to increase, the switching frequency must reduce in order to increase the gain and maintain regulation.

Figure 3 is the same gain plot as in Figure 2 only normalized with respect to the resonant frequency. This curve gives a perspective on Δf required to change the gain. It can also be noted that the steeper the gain curve, the less change in frequency to maintain regulation, and therefore the switching frequency will stay closer to resonance and flatten the efficiency curve. From an efficiency perspective, higher efficiency is achieved close to resonance.

As one makes tradeoffs through the design process, it is important to continue to go back and assess the impact on the gain profile.

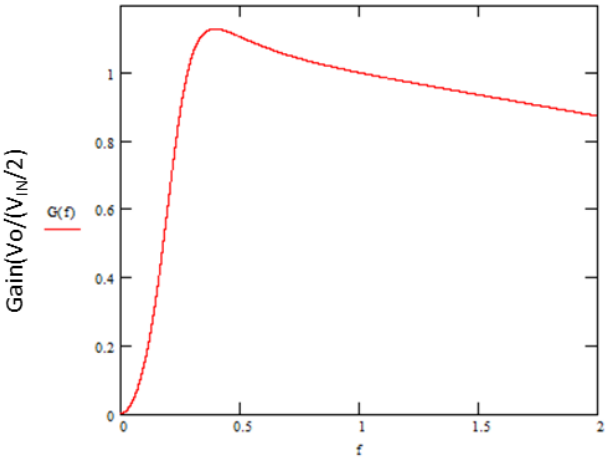

Figure 3: Gain versus normalized resonance frequency

2. LLC Converter Example

An LLC design was generated from the information provided in the Texas Instruments UCC25600 datasheet, however some deviations were made. A UCC27714 was used in place of pulse transformers for the primary half bridge gate drive, and synchronous rectification was implemented using an IR11682 synchronous rectifier controller, along with two 30V, 1 mΩ MOSFETs in place of standard diode rectification.

The primary side switches are USCi's 650V, 45 mΩ cascode in TO-220 (UJC06505T). No heatsinking is used on either of the devices.

Top line Specification:

V_{in}: 350 to 400 VDC
V_{out}: 12 VDC, 15 to 40 A

Goal: Meet Titanium 80 Plus Specification.

The highest efficiency of the Titanium 80 Plus specification is 96% at 50% load at 230VAC. It will be assumed that a bridge-less topology will be used for the front end stage, which should be optimized to 99% at the 50% load point. This would mandate an efficiency of 97% or better for the LLC stage in order to meet the Titanium specification.

A 750W to 1 kW server supply at 12 V delivers 62.5 to 83.3 A respectively, and at the 50% load mark, 31.25 to 41.7 A respectively.

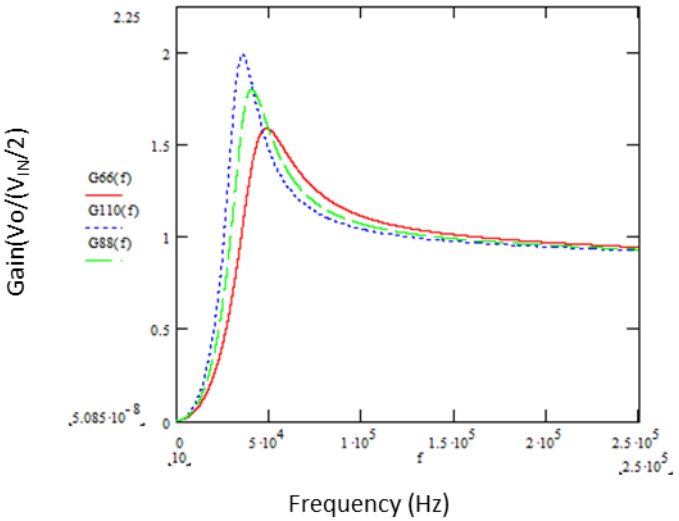

Figure 4: Gains at 35 A output

For simplicity, the design will focus on efficiency at 35 A.
Using "off the shelf" magnetics, the L_r inductance is fixed at 15.5 µH (I.C.E. 85043180), and a transformer with a primary inductance (L_m) of 195µH and a 16:1 turns ratio (I.C.Ee 85043180) was chosen. This leaves C_r to set the resonant frequency, leaving C_r and load/line as the variables influencing Q. $Q = \frac{1}{R_e} \cdot \sqrt{\frac{L_r}{C_r}}$

This highlights an important advantage of the SiC cascode; its low output capacitance C_{oss} increases Q for a given resonant inductance and it decreases the amount of time required to charge/discharge C_{oss} during switching.

In Figure 4, a gain plot for a spread of resonant frequencies (122 kHz to 157 kHz) is run for a 400 VDC input and 35 A output. The C_r capacitors in Figure 4 are 66, 88 and 110 nF, which correspond to a resonant frequency of 157 kHz, 136 kHz, and 122 kHz respectively. The UCC25600 has the ability to set a minimum switching frequency so that the converter does fall back into the "peak" of the gain plot. Setting the minimum frequency at 82 kHz, gains at the minimum frequency per the CR's produce gains of 1.2, 1.14, and 1.1. These are within an acceptable range.

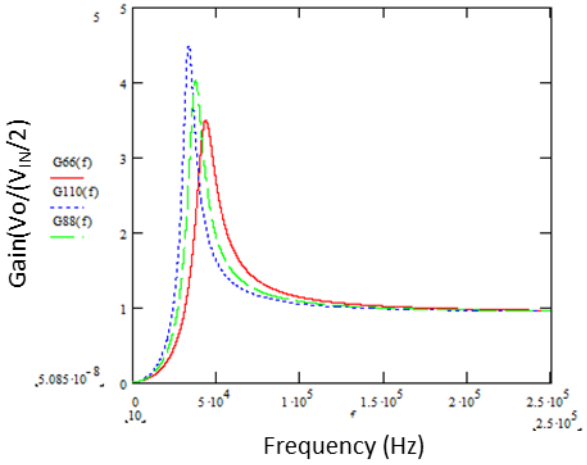

Figure 5: Gains at 15 A output

As load variation is of interest, Figure 5 is the same conditions as Figure 4 except at a load of 15 A. The peaking significantly increases as load decreases. The gains at minimal switching frequency are still within acceptable range (1.27, 1.2, and 1.1 respectively), as the slope has also increased, and therefore the gain should be higher and the converter should operate closer to resonance as the frequency drops to regulate the output.

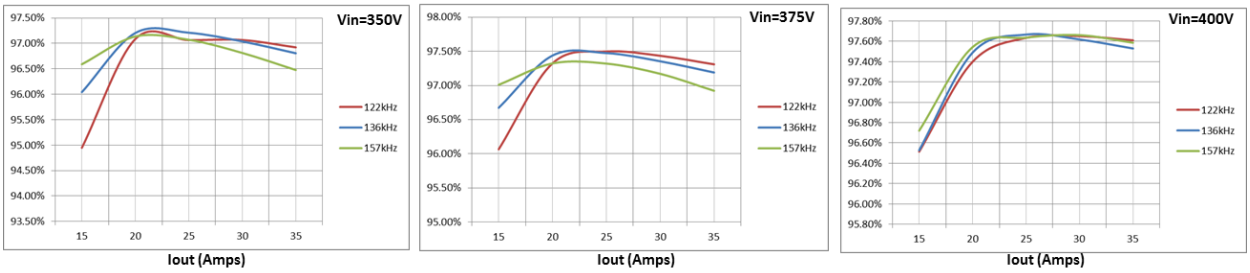

Figure 6: LLC efficiency with respect to V_{in}

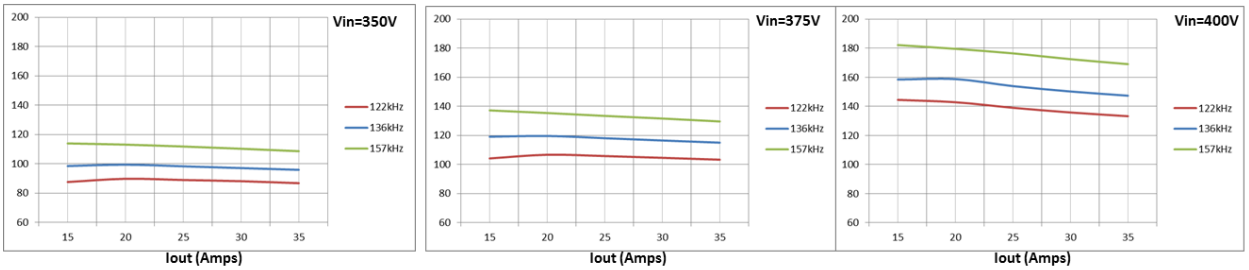

Figure 7: LLC switching frequency range (kHz)

In Figures 6 and 7 the efficiencies were run with the previous C_r/resonant frequency values across the V_{in} range (350V to 400V) and loads from 15 to 35 A. In Figure 6 the efficiencies are plotted and in Figure 7 the switching frequencies are plotted per the corresponding load current. What is readily apparent is that line variation generates a wider swing in frequencies than load variation.

From an 80 Plus perspective, all resonant points meet the 97% requirement at the 375 and 400 V input. The 350 V input technically meets the criteria set in this paper, but is probably more problematic in real life, as EMI filters and additional post regulation losses may occur in the final implementation. To regulate the output at 35 A from 350 to 400 V the switching frequency transitions from 108 kHz to 169 kHz (Δ61 kHz, f_r = 157 kHz), but to regulate the current from 15 to 35 A, the switching frequency transitions from 182 kHz to 169 kHz, (Δ13 kHz, f_r = 157 kHz).

Whereas the LLC frequency will vary widely with input voltage, in a two stage converter, the PFC can regulate the input with high precision. This makes the LLC Topology a candidate for high efficiency server supplies. As the converter operates close to resonance (zero voltage switching), switching losses on the primary side are less an obstacle, so operating at a higher input voltage can be advantageous, as can be seen in the 400 V input efficiency curve.

3. Primary Side Selection

While the secondary side typically gets all the attention in these designs, it is still important to look at the primary side switch selection. At 500 W (50% of a 1kW 80 Plus supply), 1 Watt of power dissipation equates to ~0.2% of efficiency. From a conduction loss perspective, R_{DS} can be important in picking up that extra tenth of a percent of efficiency. Using the 500 W benchmark, the difference between a 50 mΩ device and a 200 mΩ devices is a few tenths of a Watt.

The critical loss component on the primary side is switching. The design work in setting up the optimum resonance and gain still needs a device to implement the primary side function with minimal loss. The device needs to switch quickly with minimum delay as to meet the window for zero voltage switching.

In Figure 8, the low side primary side waveforms are shown. In these waveforms, the 100 mΩ, UJ3C06510TS is

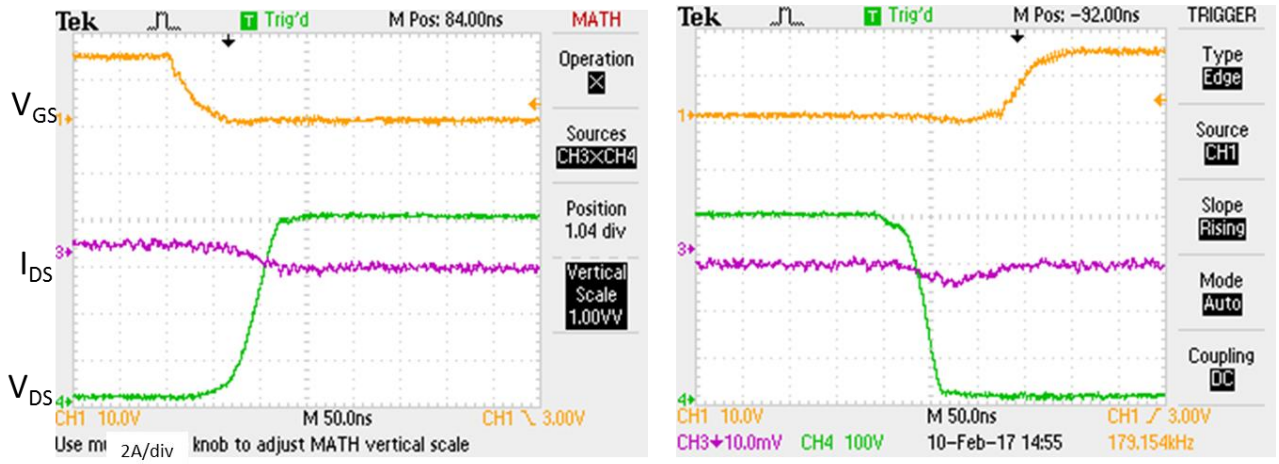

Figure 8: Primary side switching, UJ3C06510TS, 400 V_{IN}, 25 A output.

used. The waveforms are well behaved and show minimal ringing, but is zero voltage switching being achieved? In Figure 9, the waveforms above are expanded to 25 ns per division, and the Voltage and current waveforms are multiplied together to observe the energy loss.

By observing the math trace (red, $V_{DS} \cdot I_{DS}$), in a hard switched converter there would be large peaks during each transition. In the LLC, these transitions should show minimal losses occurring, and that is what is observed in in the Figure 9 math trace.

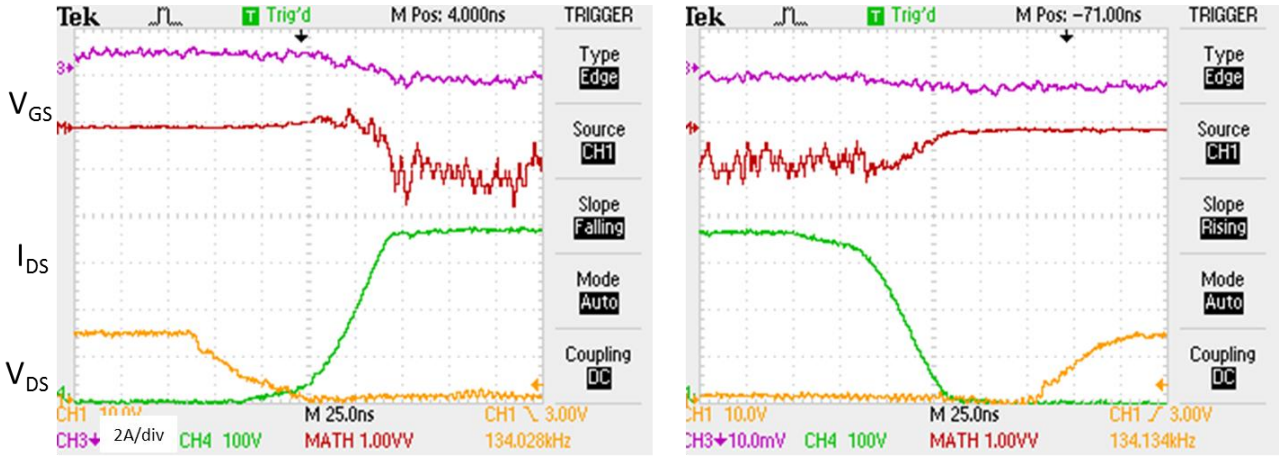

Figure 9: Primary side switching, UJ3C06510TS, 400 V_{IN}, 25 A output with $V_{DS}.I_{DS}$ math trace

4. Silicon vs. Silicon Carbide Cascode

Conventional wisdom on the LLC is to use a higher R_{DS} MOSFET to minimize the dynamic losses on the primary side, as conduction losses are minimal in comparison. With advent of the cascode device, one can get the best of both worlds. The lower R_{DS} can still be a benefit at higher power, but with the SiC cascode, one needs not sacrifice light-load efficiency due to the increase in dynamic losses associated with large die silicon devices.

In Figure 10, a 50 mΩ cascode is compared to a super-junction device of 180 mΩ. Same board, same R_G's (3 Ohm) and gate drive Voltages (0V to 14V) are used.

In a silicon comparison, one would expect the lower R_{DS} device to have lower efficiency at low load, but suffer at high load. This is not the case with a SiC cascode 650V device. The efficiency is above the silicon solution across the entire load range.

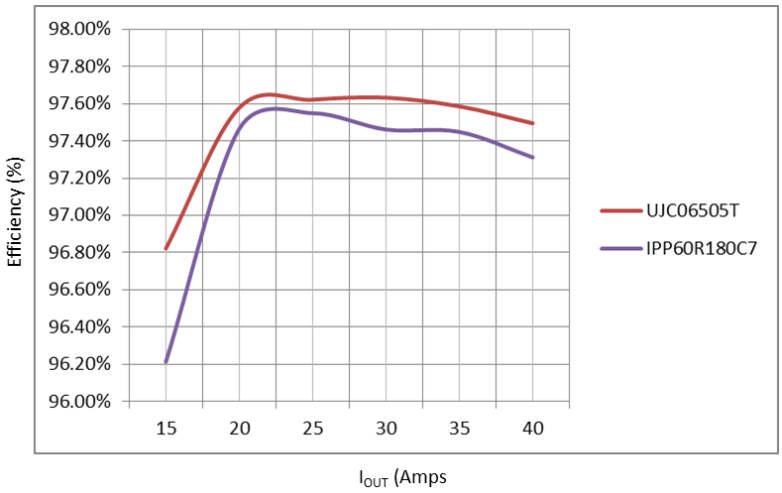

Figure 10: UJ3C06510TS, 400 V_{IN}, vs. silicon solution

The conclusion of this comparison is, in a high efficiency Titanium design, a SiC carbide cascode device is a premier primary side solution due to its superior combination of low R_{DS}, low output capacitance, and low gate charge. The low R_{DS} reduces loss at high load, and the low capacitances (gate and output) reduce dynamic losses that dominate efficiency at light-load.

5. Appendix

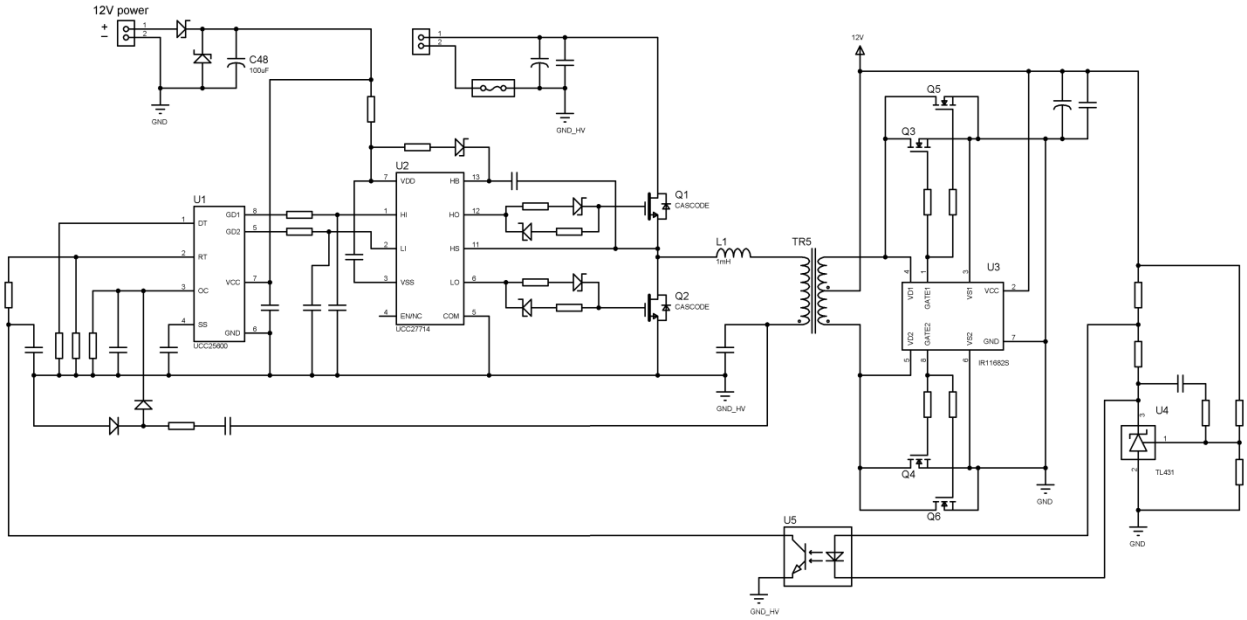

Figure 11: LLC test board schematic

6. References

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