

Figure 2. Gate Current vs. V_{GS}

As the threshold is centered at -6 Volts with a six sigma range of -4V to -10 Volts, it is a general recommendation to use -15V to insure a good stable turn off. This should account for layout inductances and less chance of accidental turn on or turn off due to high dv/dt's.

In Figure 3 a gate resistor is added to allow a +5V rail to be used in driving a JFET in a high frequency boost converter.

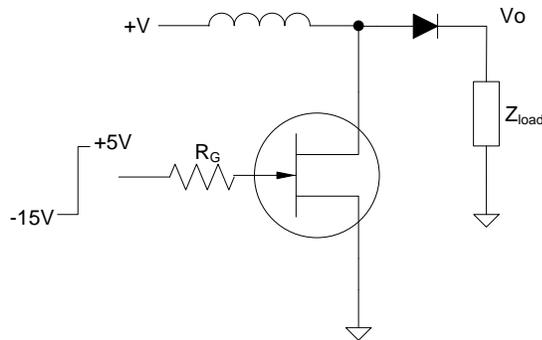


Figure 3. JFET in Boost Converter

3 Overall Device Robustness

The die of a h_{VE} JFET can be operated to 250 °C. In die form the device can be avalanche or short circuited to any energy level as long as the die temperature is kept below 250 °C, the current ratings of assembly are met and no other abs. max. values are violated.

With respect to molded packages (TO-247), for long term reliability the above applies, but the junction temperature should be kept below 175 °C.

From a die perspective, it is possible to operate above 250 °C, and once again, any systems requiring operation above these conditions, please contact h_{VE}.

4 RDS(on) with respect to Temperature

The RDS(on) of a UnitedSiC JFETs changes similarly to a high voltage silicon MOSFET with respect to temperature and current. From 25 to 175 °C the RDS(on) will increase approximately 3x in value. Figure 4 combines the current and temperature information for USCI's 1.2 kV, 45 mΩ JFET (UJN1205K).

It is important to take into account these temperature effects when calculating the system’s conduction losses.

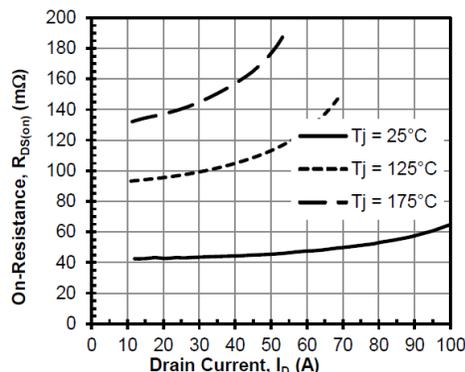


Figure 4. RDS(on) vs Drain Current vs. T_J

5 Switching Inductive Loads

The vast majority of applications using silicon carbide devices switch inductive loads. Since inductive switching can involve clamping inductive energy there are a few items to point out. The first is that the JFETs are bi-directional, so they can be utilized in synchronous rectification. Due to the dead-time loss in synchronous rectification, the addition of an anti-parallel diode may be considered.

Another option would be to operate the JFET in the cascode configuration. The cascode configuration is dealt with in another application note, so the diode inductive clamp example will be shown here.

20 A is switched through a 500μH inductor across 800 Volts using the classic inductor switching circuit shown in Figure 5. A UnitedSiC 45 mΩ 1.2 kV JFET (UJN1205K) is the switching device and 1.2 kV JBS diode (UJ2D1210T) is used to clamp the energy stored in the inductor during the off time. The 25 °C and 250 °C data are shown in Figure 6 and 7 respectively.

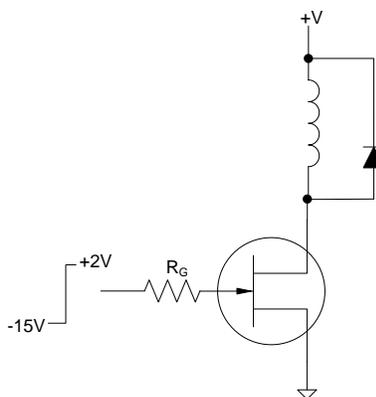


Figure 5. Inductive Switching Test

The turn on di/dt is 1.5 A/ns, and the turn off di/dt is 0.4 A/ns. This is stable across a 200 °C rise in junction temperature. The device is being driven from +2V to -15 Volts with a 4.7 Ω gate resistor.

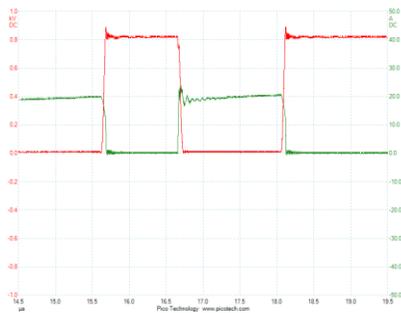


Figure 6. Inductive Switching Test 25 °C

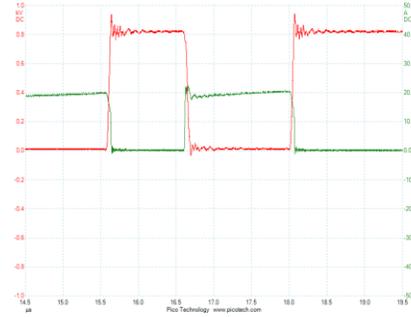


Figure 7. Inductive Switching Test 250 °C

6 Gate Charge

The previous waveforms are all generated with a simple gate drive. A resistor is used to limit the peak gate current, so as not to saturate the driver, and drive voltages are set to insure good enhancement and no accidental turn on.

Due to EMI, layout and/or load impedance, many designs require asymmetrical switching. This overview cannot go through all the options, but one of the best data sheet specifications for sizing turn on and turn off with respect to switching characteristics times are the gate charge values.

The QGS value determines the turn on delay. For the UJN1205K this is only 10nC, so the device is going to have minimum turn on time.

QGD is when the actual switching will take place, and with the UJN1205K this is 74 nC and is the plateau in the gate charge curve. Sizing the drive current for the plateau will give control over the rise and fall times. When attempting to speed up or slow down switching times, accounting for QGD will deliver the best design.

The remaining charge to reach QG is directly related to better enhancement and turn off delay. In the UJN1205K, the remaining 23nC is tied to the turn off delay. With symmetrical drive currents, turn off delay will be about twice the turn on delay.

7 Conclusion

This application note is an overview of United Silicon Carbide's 1.2 kV normally on JFETs. They can be operated over a wide range of gate voltages, and their high temperature capability makes them extremely rugged.