APPLICATION NOTE
UnitedSiC_AN0027 – March 2021

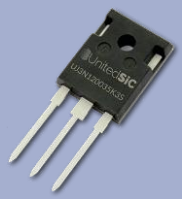
ESD Ratings of UnitedSiC FETs and JFETs

By William Simon, Ph.D.

Introduction

This Application Note discusses the ESD capabilities of UnitedSiC's transistor offerings.

Dr. William Simon is the New Product Introduction Manager at UnitedSiC. He received his Ph.D. in Materials Engineering from Rutgers University in 2006, and has 15 years experience in Power and RF Semiconductor Processing.



Learn more about power electronic applications at https://unitedsic.com/downloads

ESD rating of SiC FETs

UnitedSiC cascode FETs utilize a low voltage MOSFET to turn the Normally-On JFET to a Normally-Off device with the Gate drive behavior of a Silicon MOSFET.

UnitedSiC's FET product line is built on the core technology of a High-Voltage, Normally-On SiC JFET coupled with a Low Voltage, Normally-Off Silicon MOSFET in a cascode configuration. Given the cascode configuration of the SiC JFET and Si MOSFET, the MOSFET is connected to the Gate and Source pins of a package, and it the limiting device when it comes to ESD capability. The JFETs are p-n junctions and can handle far more ESD than the MOSFET. Our MOSFETs use integrated diodes as ESD protection, and the size and capacitance of the MOSFET become the determining factor in ESD capability.

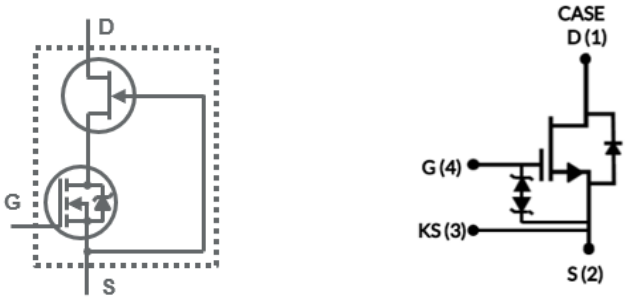


Figure 1: *(left)* Basic Cascode diagram showing the MOSFET drain connected to the JFET source. *(right)* Cascode diagram showing back-to-back diodes on the Gate to Source pads of the MOSFET.

Across the UnitedSiC SiC FET product lines we use a family of MOSFETs that are scaled to the size and RDSon of the JFET. The smallest JFETs will require the smallest MOSFETs, and these become the limiting ESD ratings for our parts. This also means by ESD testing the MOSFETs alone, we determine the ESD ratings of all products that use that MOSFET.

For the Charged Device Model samples of every MOSFET were tested up to ±2000V and passed. This puts the parts into CDM class C3 (>1000V). For Human Body Model testing, samples of every MOSFET were tested up to ±8000V on each of the 3 pin combinations. All MOSFETs passed to 8000V for the Drain to Source pin pair. Gate to Source and Gate to Drain testing varied from device size. The smallest MOSFETs passed at Gate-to-Source at 3900V and Gate-to-Drain at 3700V. This sets the minimum HBM class H2 (>2000V to <4000V) for all UnitedSiC devices.

P/N	CDM		HBM			
	Class	results	Class	G to S	G to D	D to S
AW1044	C3	±2kV	3B	8kV	8kV	8kV
AW1046	C3	±2kV	2	3.9kV	3.7kV	8kV
AW1048	C3	±2kV	3A	4.9kV	4.6kV	8kV
AW1060	C3	±2kV	3B	8kV	8kV	8kV
AW1065	C3	±2kV	3A	4.8kV	4.9kV	8kV

Table 1 ESD Results for MOSFETs

The Larger SiC FETs with larger MOSFETs will outperform the H2 classification. The two largest devices, are rated to class 3B (>8000V).

ESD Rating of SiC JFETs

Similar to the MOSFETs, the UnitedSiC family of SiC JFETs are scaled with size and the smallest devices are the most sensitive to ESD. Unlike the MOSFETs, the JFET is fundamentally insensitive to ESD because the device is made up of p-n junctions. Utilizing the smallest JFET in the lineup, Charged Device Model testing was done to ±1000V, and Human Body Model testing for all pin pairs was done to ±8000V. Putting all JFETs in the C3 and H3A classes, respectively.

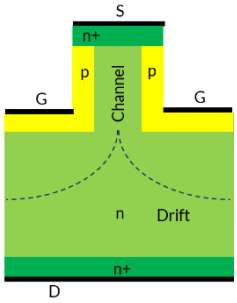


Figure 2: Unit cell of JFET structure highlighting (a) the lack of gate oxide, and (b) the 2 p-n junctions (Gate-to-Drain, and Gate-to-Source).