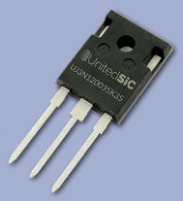
APPLICATION NOTE
UnitedSiC_AN0031 – March 2022

Improvements in On-board Charger Performance Using the Latest SiC FET Technology

By Anup Bhalla, Pete Losee, Zhongda Li, Deborah Sumaoang, Ke Zhu, Jonathan Dodge

Abstract

Silicon Carbide FETs have already established themselves in on-board charger (OBC) circuits, especially for cases when battery operating voltages exceed 500V. The low power losses of these devices allow both through-hole and surface mount packages to be employed in this application. We will examine the relative thermal performance of these package options, and demonstrate the viability of the TO247-4L and D2PAK-7L options in 6.6 kW and 22 kW chargers.



Learn more about power electronic applications at https://unitedsic.com/application-notes/

Introduction

Silicon Carbide FETs are widely used in on-board chargers (OBC) and DC/DC converters in battery electric vehicles (EVs) [1]. Their use in traction inverters is also rapidly growing. They become the device of choice when the system bus voltages exceed 500 V (e.g., 800 V), because they switch much faster than IGBTs. They are also an excellent choice when hard switching is required in the PFC circuit of lower bus voltage systems, since their diode recovery performance is much better than that of silicon superjunction FETs, and therefore allow for higher frequency switching and lower losses. Finally, the growing trend of making these chargers bidirectional in energy flow, to allow vehicle to grid power transfer, is enabled by the same properties of these wide bandgap devices.

The on-board charger performs a conversion of the input 1 or 3 phase AC into a DC rail, followed by a DC/DC conversion to charge the car battery. In charging mode, the front-end acts as a rectifier and uses a totem-pole PFC, or at higher power an active front-end. These circuits can be operated to reverse the power flow, i.e., as inverters. The DC/DC topology selected for charging can be the LLC or CLLC type, the latter being well suited to bidirectional power transfer. The DC rail may also support another LLC converter at lower power to supply the 12 V electronics in the EV. If bidirectional energy flow is not needed, the Vienna rectifier is a frequent choice for the PFC rectifier.

SiC device technology and package options

Figure 1 shows the state of the art in commercially available unipolar power semiconductors [2]. The continuous progress in device technology in the last decade has resulted in the Gen 4 SiC JFET and SiC FET (cascode), shown by the blue symbols in that figure. A low $R_{ds}A$ at a given rating allows lower resistance in the same package. It also allows a lower die size and capacitance for a given on-resistance, enabling lower switching losses as well.

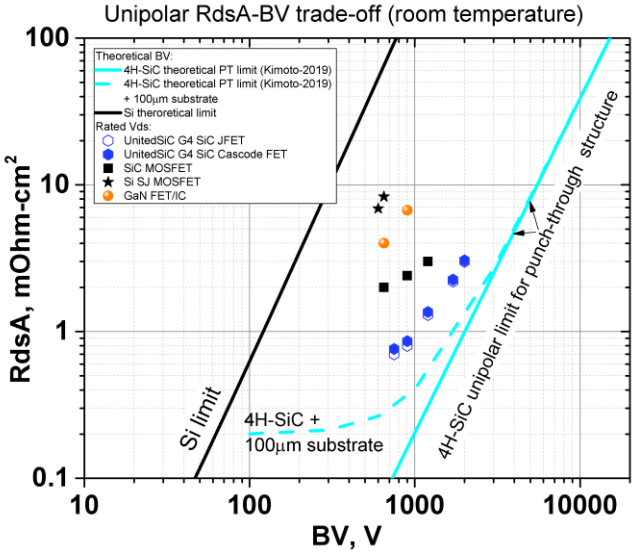


Figure 1: RdsA vs Voltage rating of state-of-the-art Silicon and Wide Bandgap switch technologies in 2021.

Figure 2 shows the package options discussed in this paper. The TO247-4L is a widely available variant of the TO247 package. The D2PAK-7L is a surface mount package popular with silicon carbide devices. The through-hole TO247 can dissipate more power, given the large, exposed

copper tab. The D2PAK-7L die pad is relatively small, given the need to maintain a high creepage distance. Table 1 shows a comparison of relevant parameters, including typical package inductance, heat pad size (area of copper connected to the heatsink), creepage and clearance.

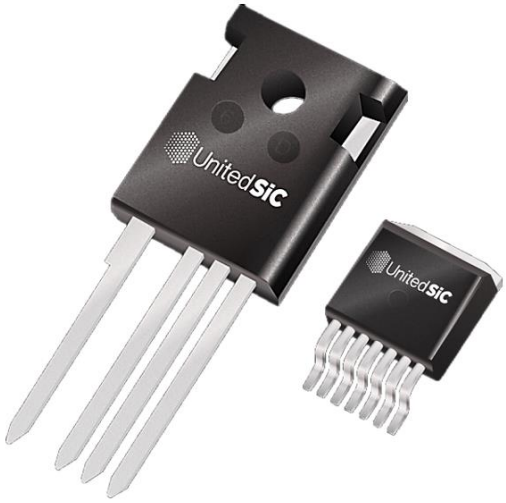


Figure 2: The TO247-4L (left) and D2PAK-7L (right) are popular packages for through-hole and surface mount options in on-board chargers.

The use of SMT devices can simplify and increase manufacturing automation. Therefore, the option of using the D2PAK-7L on an insulated metal substrate (IMS) as an alternative to the TO247-4L in the liquid cooled environment of an EV is worthy of analysis.

Since the analysis of power losses and peak temperature rise require device conduction loss data, switching loss data and thermal resistance data, we will examine that first. Then the FET-Jet [3] online calculator is used to extract the operating worst case losses and temperature rise to check the viability of a selected device and package combination.

The switching data as a function of current has been entered into the calculator based on datasheet curves (see figures 3a and 3b), along with the temperature dependent on-resistance for all the devices considered. The typical and worst-case thermal resistance (R_{thJC}) is also available within the calculator. Next, we look at simulations to guide reasonable estimates of R_{thCA} to complete the dataset needed for this analysis.

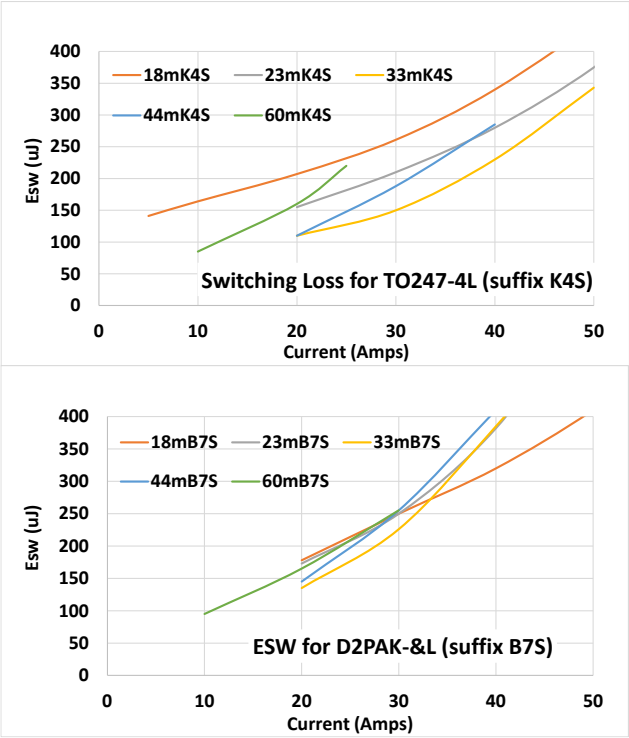


Figure 3a (top) is the switching loss vs current at 400V bus for TO247-4L 750V G4 SiC FETs. Figure 3b (bottom) is the same data for the devices in D2PAK-7L.

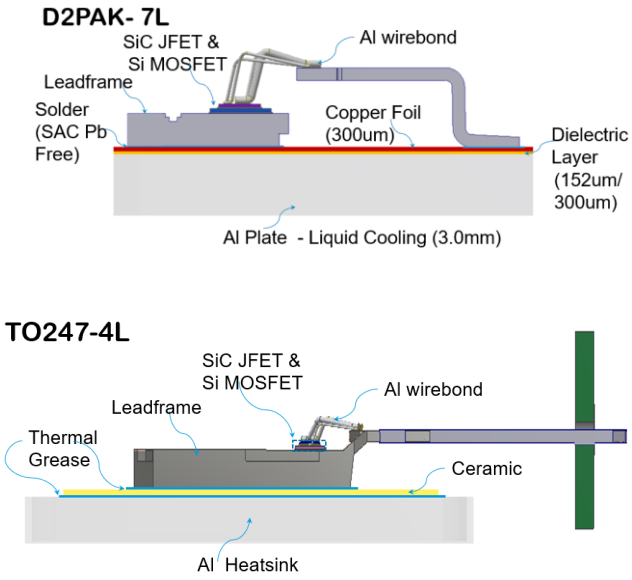


Figure 4: Visualizing the thermal path for the TO247-4L and D2Pak-7L from the junction to the coolant fluid.

Package	Die Pad	Inductance	Creepage	Clearance
	mm2	nH	mm	mm
D2PAK-7L	43	3 to 5	6.7	6.1
TO247-4L	176	10 to 15	3.9	3.9

Table 1: Comparison of the two packages shown in Figure 2. The SMT device clearly has lower inductance, but also a smaller area of heat removal.

Simulated comparison of typical thermal environments

Figure 4 shows a typical usage view of the totem-pole PFC using the TO247-4L and that using the D2PAK-7L on IMS, showing the heat flow path from the device junction to the fluid used to cool the power electronics. Table 2a and 2b summarize the junction-to-case and case-to-fluid thermal resistance of each device for a range of thermal interface (TIM) isolation options.

Device	Ceramic Isolator Material	RthJC	RthJ-to-Fluid
	AL2O3	0.433°C/W	0.813°C/W
UJ4SC075018K4S	SI3N4	0.430°C/W	0.750°C/W
	ALN	0.426°C/W	0.652°C/W
	AL2O3	0.650°C/W	1.059°C/W
UJ4C075044K4S	SI3N4	0.641°C/W	0.994°C/W
	ALN	0.639°C/W	0.986°C/W

Table 2a: Thermal resistance performance for TO247 based devices mounted to coldplates with ceramic isolators.

Device	IMS Dielectric Thk Thermal Cond	RthJC @ 75°C	RthJ-to-IMS @ @ 75°C
UJ4C075044B7S	150um, 3W/mk	0.908 °C/W	1.766 °C/W
UJ4C075044B7S	300um, 5W/mk	0.906 °C/W	2.004 °C/W
UJ4SC075018B7S	150um, 3W/mk	0.438 °C/W	1.299 °C/W
UJ4SC075018B7S	300um, 5W/mk	0.387 °C/W	1.348 °C/W

Table 2b: Thermal resistance performance for D2PAK-7L devices built on IMS, where the bottom 3mm Al is liquid cooled.

Based on these results, we can use 0.6 °C/W for TO247 and 1.2 °C/W for D2Pak-7L as a median for the thermal resistance from the case to the fluid – added to the junction case thermal resistance. Despite the small chip size of the SiC FETs, low R_{thJC} within the package is achieved via silver sintered die attach.

Case 1: 6.6kW (AC/DC) totem pole PFC for a 400V bus system

Figure 5 shows the basic circuit for the totem pole PFC topology. Table 3 shows a compilation of power loss and temperature rises for the 6.6 kW using a range of Gen 4 devices for this application at full load. Other circuit conditions are 230 Vrms input, 400 V DC rail, 75 kHz CCM mode switching, 20% inductor ripple, heatsink/fluid temperature 80 °C, using a fixed 11 mΩ, 750 V device on the slow leg in the same package type, and varying the devices for the two interleaved fast legs of the totem pole PFC [4]. We can see a range of options for the fast leg, from 18 mΩ to 60 mΩ with the lowest $R_{ds(on)}$ device offering the highest performance. The table shows the worst-case power loss per fast leg FET, expected junction temperature, and the semiconductor efficiency, which is a measure of the efficiency loss from just the power

semiconductors. Even with the higher case-to-fluid thermal resistance of 1.2 °C/W, the surface mount options shown in the table below are all reasonable choices. The final part decision can be based on overall thermal, efficiency, and cost constraints in the design, with many device options now offered by Qorvo.

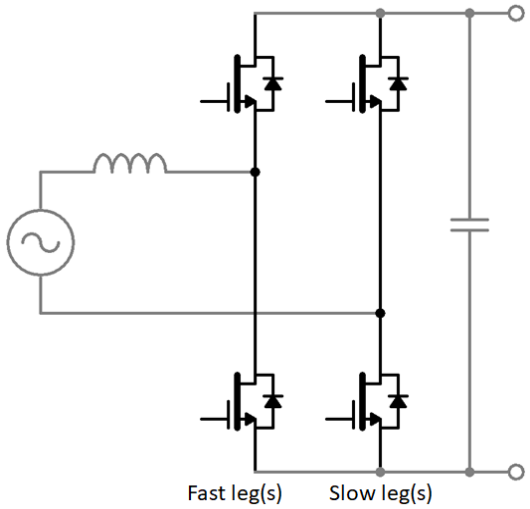


Figure 5: Totem-pole PFC topology used in this analysis. We assume two interleaved fast legs with one switch per position and single low Rds device in the slow leg.

Device Fast Legs	Device Rating	Package	Loss/FET W	Tj pk C	Semicon Efficiency
UJ4C075018K4S	18m, 750V	TO247-4L	8.3	88	99.3%
UJ4C075023K4S	23m, 750V	TO247-4L	8.6	89	99.3%
UJ4C075033K4S	33m, 750V	TO247-4L	8.9	91	99.3%
UJ4C075044K4S	44m, 750V	TO247-4L	10.3	94	99.2%
UJ4C075060K4S	60m, 750V	TO247-4L	13.5	101	99.0%
UJ4SC075018B7S	18m, 750V	D2PAK-7L	6.8	91	99.4%
UJ4SC075023B7S	23m, 750V	D2PAK-7L	8.6	97	99.3%
UJ4SC075033B7S	33m, 750V	D2PAK-7L	9.9	101	99.2%
UJ4SC075044B7S	44m, 750V	D2PAK-7L	10.5	104	99.2%
UJ4SC075060B7S	60m, 750V	D2PAK-7L	13.7	109	99.0%

Table 3: Calculated losses in the fast-switching FET, peak junction temperature and semiconductor loss limited efficiency for various G4 SiC FET options 6.6 kW TPPFC operating at 75 kHz.

Case 2: 6.6 kW CLLC DC/DC for a 400V bus system

We can now consider the same series of devices for what they deliver in the CLLC stage of the on-board charger. In general, losses are lower since the devices are not hard switching. Here we assume a full-bridge CLLC implementation, as shown in Figure 6, and examine power losses for the different options at 6.6 kW, 400 V bus, switching at 300 kHz, with the coolant fluid temperature at 80 °C, and the same assumption of 0.6 °C/W for TO247-4L and 1.2 °C/W for D2PAK-7L IMS as the additional case-to-fluid thermal impedance. Losses computed for the primary side FETs are listed in Table 4.

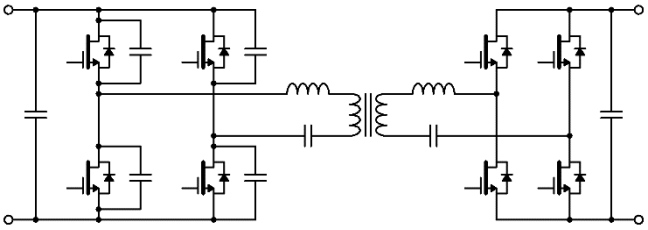


Figure 6. CLLC topology used for the estimates in Table 5. The primary side FETs are considered. The same devices can often be used on the secondary side.

Device	Device Rating	Package	Loss/FET W	Tj pk C	Semicon Efficiency
UJ4C075018K4S	18m, 750V	TO247-4L	4.1	84	99.8%
UJ4C075023K4S	23m, 750V	TO247-4L	5.2	86	99.7%
UJ4C075033K4S	33m, 750V	TO247-4L	7.9	90	99.5%
UJ4C075044K4S	44m, 750V	TO247-4L	10.7	94	99.4%
UJ4C075060K4S	60m, 750V	TO247-4L	15.3	104	99.1%
UJ4SC075018B7S	18m, 750V	D2PAK-7L	4.2	87	99.8%
UJ4SC075023B7S	23m, 750V	D2PAK-7L	5.3	90	99.7%
UJ4SC075033B7S	33m, 750V	D2PAK-7L	8.2	97	99.5%
UJ4SC075044B7S	40m, 750V	D2PAK-7L	11.4	106	99.3%
UJ4SC075060B7S	60m, 750V	D2PAK-7L	16.4	115	99.0%

Table 4: Calculated losses in the primary side FETs, peak junction temperature and semiconductor loss limited efficiency for various G4 SiC FET options. 6.6 kW full-bridge CLLC operating at 300 kHz.

In this case, switching losses are much lower despite the higher frequency, which is the benefit of nearly lossless switching in LLC circuits. In addition, there are many viable options for designers to choose from, both for through hole and surface mount, providing flexibility to optimize performance, thermal management, board space and cost. It is also useful that SiC FETs can be driven with 0 to 10 V drives within minimal impact on performance, which helps limit driver losses.

Case 3: 22 kW Vienna rectifier

A final useful example is using the 750 V platform in a 22 kW Vienna rectifier shown in figure 7. For this 3-phase circuit, we perform the calculations assuming the use of 750 V FETs and 50 A, 1200 V UJ3D1250K2 diodes. We assume 230 V rms AC input, 3-phase, an 800 V bus, 40 kHz switching and the same thermal case to ambient conditions for the through-hole and SMT options as in the previous examples. For 22 kW input, RMS phase currents are about 31.9 A.

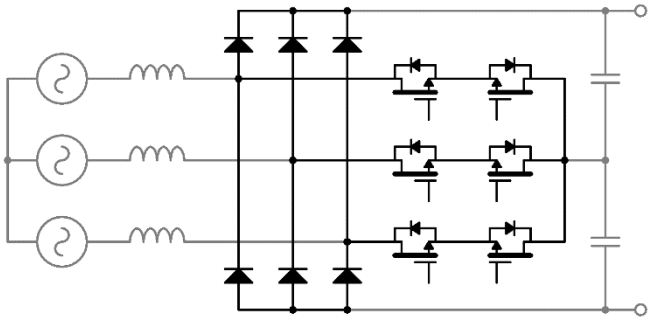


Figure 7. Vienna rectifier using all SiC devices. The diodes are 1200 V SiC diodes, while the FETs are Gen 4 750 V SiC FETs.

Device	Device Rating	Package	Loss/FET W	Tj pk C	Semicon Efficiency
UJ4C075018K4S	18m, 750V	TO247-4L	14.3	94	99.2%
UJ4C075023K4S	23m, 750V	TO247-4L	14	95	99.2%
UJ4C075033K4S	33m, 750V	TO247-4L	19.5	104	99.1%
UJ4C075044K4S	44m, 750V	TO247-4L	26.4	115	98.9%
UJ4SC075018B7S	18m, 750V	D2PAK-7L	10.7	97	99.3%
UJ4SC075023B7S	23m, 750V	D2PAK-7L	15.5	110	99.2%
UJ4SC075033B7S	33m, 750V	D2PAK-7L	23.2	129	99.0%
UJ4SC075044B7S	44m, 750V	D2PAK-7L	32.7	155	98.7%

Table 5: Calculated losses in FETs, peak junction temperature and semiconductor loss limited efficiency for various G4 SiC FET options. 22 kW Vienna rectifier, 800 V Bus, 40 kHz.

In this case, the ability to dissipate more power in the TO247-4L package plays a larger role, and higher resistance devices can be used with good thermal margin. On the other hand, losses are so low in the 18 mΩ to 33 mΩ devices, that they offer a viable surface mount option even at this power level.

Conclusion

The performance improvements of Gen 4 SiC FETs and the availability of a wide range of $R_{ds(on)}$ classes in both through-hole and surface mount packages allows designers to keep improving on-board charger designs in efficiency, size, and waste heat, while keeping costs low. Furthermore, using simpler 0 to 10/12/15 V gate drive helps manage cost and complexity.

References

[1] J. Yuan et. al, "A review of bidirectional on-board chargers for electric vehicles", IEEE Access, 2021, Vol. 9
[2] A. Bhalla, "750V Gen 4 SiC FETs Enable Higher Efficiency Power Designs", Bodo's Power Systems, Jan 2021, pp. 18-22
[3] https://info.unitedsic.com/fet-jet
[4] K. Zhu, "Enabling 99.3% efficiency in 3.6kW Totem-pole PFC using new 750V Gen 4 SiC FETs", Qorvo application note AN0026, March 2021