

DATASHEET

UF3N090800Z

900V-735mΩ SiC Normally-on JFET

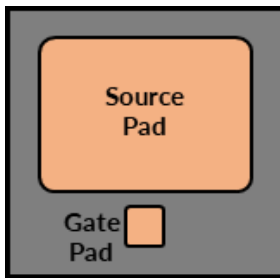
Preliminary, March 2019

Description

United Silicon Carbide, Inc offers the high-performance G3 SiC normally-on JFET transistors. This series exhibits ultra-low on resistance ($R_{DS(ON)}$) and gate charge (Q_G) allowing for low conduction and switching loss. The device normally-on characteristics with low $R_{DS(ON)}$ at $V_{GS} = 0\text{ V}$ is also ideal for current protection circuits without the need for active control, as well as for cascode operation.

Features

- ◆ Typical on-resistance $R_{DS(on),typ}$ of 735mΩ
- ◆ Voltage controlled
- ◆ Maximum operating temperature of 175°C
- ◆ Extremely fast switching not dependent on temperature
- ◆ Low gate charge
- ◆ Low intrinsic capacitance
- ◆ RoHS compliant



Typical applications

- ◆ Over Current Protection Circuits
- ◆ DC-AC Inverters
- ◆ Switch mode power supplies
- ◆ Power factor correction modules
- ◆ Motor drives
- ◆ Induction heating

Part Number	Package
UF3N090800Z	Die on tape
UF3N090800	Undiced wafer



Maximum Ratings

Parameter	Symbol	Test Conditions	Value	Units
Drain-source voltage	V_{DS}		900	V
Gate-source voltage	V_{GS}	DC	-20 to +3	V
		AC ¹	-20 to +20	V
Continuous drain current ^{2,3}	I_D	$T_C = 25^\circ\text{C}$	4.8	A
		$T_C = 100^\circ\text{C}$	3.4	A
Pulsed drain current ^{3,4}	I_{DM}	$T_C = 25^\circ\text{C}$	TBD	A
Maximum junction temperature ⁵	$T_{J,max}$		175	$^\circ\text{C}$
Operating and storage temperature	T_J, T_{STG}		-55 to 175	$^\circ\text{C}$

1. +20V AC rating applies for turn-on pulses <200ns applied with external $R_G > 1\Omega$.

2. Limited by $T_{J,max}$

3. Assumes a maximum junction-to-case thermal resistance of 2.9°C/W

4. Pulse width t_p limited by $T_{J,max}$

5. Package limited

Electrical Characteristics ($T_J = +25^\circ\text{C}$ unless otherwise specified)

Typical Performance - Static

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Drain-source breakdown voltage	BV_{DS}	$V_{GS} = -20\text{V}, I_D = 1\text{mA}$	900			V
Total drain leakage current	I_{DSS}	$V_{DS} = 900\text{V}, V_{GS} = -20\text{V}, T_J = 25^\circ\text{C}$		0.8	5	μA
		$V_{DS} = 900\text{V}, V_{GS} = -20\text{V}, T_J = 175^\circ\text{C}$		TBD		
Total gate leakage current	I_{GSS}	$V_{GS} = -20\text{V}, T_J = 25^\circ\text{C}$		0.03	0.5	μA
		$V_{GS} = -20\text{V}, T_J = 175^\circ\text{C}$		TBD		μA
Drain-source on-resistance	$R_{DS(on)}$	$V_{GS} = 2\text{V}, I_D = 1\text{A}, T_J = 25^\circ\text{C}$		598		m Ω
		$V_{GS} = 0\text{V}, I_D = 1\text{A}, T_J = 25^\circ\text{C}$		735	1000	
		$V_{GS} = 2\text{V}, I_D = 1\text{A}, T_J = 175^\circ\text{C}$		TBD		
		$V_{GS} = 0\text{V}, I_D = 1\text{A}, T_J = 175^\circ\text{C}$		TBD		
Gate threshold voltage	$V_{G(th)}$	$V_{DS} = 5\text{V}, I_D = 2.4\text{mA}$	-11	-9	-7	V
Gate resistance	R_G	f=1MHz, open drain		13		Ω

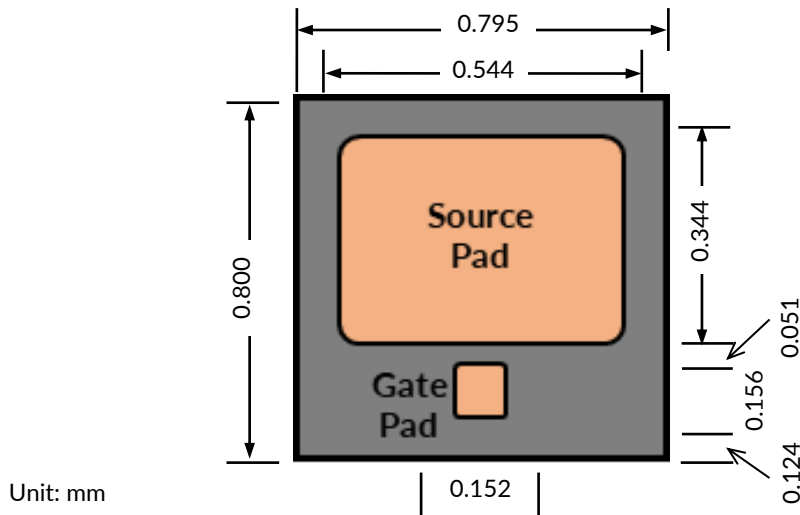
Typical Performance - Dynamic

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Input capacitance	C_{iss}	$V_{DS}=100V, V_{GS}=-20V$ $f=100kHz$		80.2		pF
Output capacitance	C_{oss}			12.8		
Reverse transfer capacitance	C_{rss}			9.6		
Effective output capacitance, energy related	$C_{oss(er)}$	$V_{DS}=0V$ to 600V, $V_{GS}=-20V$		9		pF
C_{oss} stored energy	E_{oss}	$V_{DS}=600V, V_{GS}=-20V$		1.62		μJ
Total gate charge	Q_G	$V_{DS}=600V, I_D=3.5A,$ $V_{GS} = -18V$ to 0V		TBD		nC
Gate-drain charge	Q_{GD}			TBD		
Gate-source charge	Q_{GS}			TBD		
Turn-on delay time	$t_{d(on)}$	$V_{DS}=600V, I_D=3.5A,$ Gate Driver = -18V to 0V, $R_G=1\Omega,$ Inductive Load, FWD: UJ3D1202TS $T_J=25^\circ C$		TBD		ns
Rise time	t_r			TBD		
Turn-off delay time	$t_{d(off)}$			TBD		
Fall time	t_f			TBD		
Turn-on energy	E_{ON}			TBD		
Turn-off energy	E_{OFF}	$V_{DS}=600V, I_D=3.5A,$ Gate Driver = -18V to 0V, $R_G=1\Omega,$ Inductive Load, FWD: UJ3D1202TS $T_J=150^\circ C$		TBD		μJ
Total switching energy	E_{TOTAL}			TBD		
Turn-on delay time	$t_{d(on)}$			TBD		
Rise time	t_r			TBD		
Turn-off delay time	$t_{d(off)}$			TBD		
Fall time	t_f			TBD		
Turn-on energy	E_{ON}			TBD		
Turn-off energy	E_{OFF}		TBD			
Total switching energy	E_{TOTAL}		TBD			

Mechanical Characteristics

Parameter	Typical Value	Units
Die dimensions with scribe line (L x W)	0.795 x 0.800	mm
Scribe line width	80	μm
Source pad metal dimensions (L x W)	0.544 x 0.344	mm
Gate pad metal dimensions (L x W)	0.152 x 0.156	mm
Source metallization (AlCu)	5	μm
Gate metallization (AlCu)	5	μm
Backside drain metallization (Ti/Ni/Ag)	0.1/0.2/1	μm
Frontside passivation	Polyimide	
Die thickness	150	μm
Wafer size	150	mm
Gross die per wafer	22938	

Chip Dimensions



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