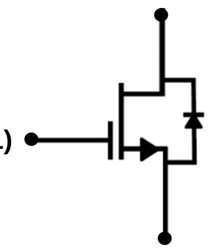
Description

United Silicon Carbide's cascode products co-package its xJ series high-performance SiC JFETs with a cascode optimized MOSFET to produce the only standard gate drive SiC device in the market today. This series exhibits ultra-low gate charge, but also the best reverse recovery characteristics of any device of similar ratings. These devices are excellent for switching inductive loads, and any application requiring standard gate drive.

CASE

1 2 3



Part Number	Package	Marking
UJC06505K	TO-247-3L	UJC06505K

Features

- Max. on-resistance $R_{DS(on)max}$ of 45mΩ
- Standard 12V gate drive
- Maximum operating temperature of 150°C
- Excellent reverse recovery
- Low gate charge
- Low intrinsic capacitance
- RoHS compliant

Typical Applications

- EV charging
- PV inverters
- Switch mode power supplies
- Power factor correction modules
- Motor drives
- Induction heating

Maximum Ratings

Parameter	Symbol	Test Conditions	Value	Units
Drain-source voltage	V_{DS}		650	V
Gate-source voltage	V_{GS}	DC	-25 to +25	V
Continuous drain current [1]	I_D	T_C = 25°C	36.5	A
		T_C = 100°C	23.5	A
Pulsed drain current [2]	I_{DM}	T_C = 25°C	113	A
Short-circuit withstand time [3]	t_{SC}	V_{GS}=15V, V_{DS}<300V	4	μs
Single pulsed avalanche energy [3]	E_{AS}	L=15mH, I_{AS} =2.5A	52	mJ
Power dissipation	P_{tot}	T_C = 25°C	113	W
Maximum junction temperature	$T_{J,max}$		150	°C
Operating and storage temperature	T_J, T_{STG}		-55 to 150	°C
Max. lead temperature for soldering, 1/8" from case for 5 Seconds	T_L		250	°C

1 Limited by $T_{J,max}$

2 Pulse width t_p limited by $T_{J,max}$

3 Starting T_J = 25°C

Electrical Characteristics (T_J = +25°C unless otherwise specified)

Typical Performance - Static

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Drain-source breakdown voltage	BV_{DS}	V_{GS}=0V, I_D=1mA	650			V
Total drain leakage current	I_{DSS}	V_{DS} = 650V, V_{GS} = 0V, T_J = 25°C		25	500	μA
		V_{DS} = 650V, V_{GS} = 0V, T_J = 150°C		65		
Total gate leakage current	I_{GSS}	V_{DS}=0V, T_j=25°C, V_{GS} = -20V / +20V		5	100	nA
Drain-source on-resistance	$R_{DS(on)}$	V_{GS}=12V, I_D=25A, T_J = 25°C		34	45	mΩ
		V_{GS}=12V, I_D=25A, T_J = 150°C		62		
Gate threshold voltage	$V_{G(th)}$	V_{DS} = 5V, I_D = 10mA	4.5	5	5.5	V
Gate resistance	R_G	f = 1MHz, open drain		1.1		Ω

Typical Performance - Reverse Diode

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Diode continuous forward current [1]	I_S	T_C = 25°C			36.5	A
Diode pulse current [2]	$I_{S,pulse}$	T_C = 25°C			113	A
Forward voltage	V_{FSD}	V_{GS} = 0V, I_F =25A, T_J = 25°C		1.55	2	V
		V_{GS} = 0V, I_F = 25A, T_J =150°C		1.9		
Reverse recovery charge	Q_{rr}	V_R=400V, I_F=25A, V_{GS} =0V, di/dt=1200A/μs, T_J = 25°C		85		nC
Reverse recovery time	t_{rr}			30		ns
Reverse recovery charge	Q_{rr}	V_R=400V, I_F=25A, V_{GS} =0V, di/dt=1200A/μs, T_J = 150°C		95		nC
Reverse recovery time	t_{rr}			33		ns

Typical Performance - Dynamic

Parameter	symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Input capacitance	C_{iss}	V_{DS} = 400V, V_{GS} = 0V, f = 100kHz		2107		pF
Output capacitance	C_{oss}			80		
Reverse transfer capacitance	C_{rss}			5.7		
Effective output capacitance, energy related	$C_{oss(er)}$	V_{DS} = 0V to 400V, V_{GS} = 0V		100		pF
Effective output capacitance, time related	$C_{oss(tr)}$	V_{DS} = 0V to 400V, V_{GS} = 0V		181		pF
C_{OSS} stored energy	E_{oss}	V_{DS} = 400V, V_{GS} = 0V		8		μJ
Total gate charge	Q_G	V_{DS}=400V, I_D = 25A, V_{GS}=0V to 12V		47.5		nC
Gate-drain charge	Q_{GD}			15		
Gate-source charge	Q_{GS}			15		
Turn-on delay time	$t_{d(on)}$	V_{DS}=400V, I_D=25A, Gate Driver = 0V to +12V, Turn-on $R_{G,EXT}$ = 0Ω, Turn-off $R_{G,EXT}$ = 20Ω Inductive Load, FWD: UJD06520T T_J = 25°C		29		ns
Rise time	t_r			10		
Turn-off delay time	$t_{d(off)}$			70		
Fall time	t_f			15		
Turn-on energy	E_{ON}			196		μJ
Turn-off energy	E_{OFF}			101		
Total switching energy	E_{TOTAL}			297		
Turn-on delay time	$t_{d(on)}$	V_{DS}=400V, I_D=25A, Gate Driver = 0V to +12V, Turn-on $R_{G,EXT}$ = 0Ω, Turn-off $R_{G,EXT}$ = 20Ω Inductive Load, FWD: UJD06520T T_J = 150°C		31		ns
Rise time	t_r			14		
Turn-off delay time	$t_{d(off)}$			78		
Fall time	t_f			17		
Turn-on energy	E_{ON}			215		μJ
Turn-off energy	E_{OFF}			124		
Total switching energy	E_{TOTAL}			339		

Thermal Characteristics

Parameter	symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Thermal resistance, junction-to-case	$R_{\theta JC}$			0.84	1.1	°C/W

Typical Performance Diagrams

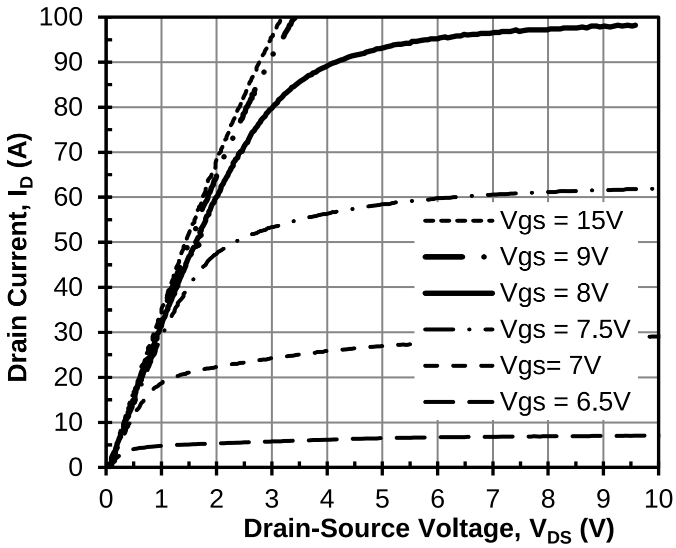


Figure 1 Typical output characteristics at T_j = - 55°C, tp < 250 μs

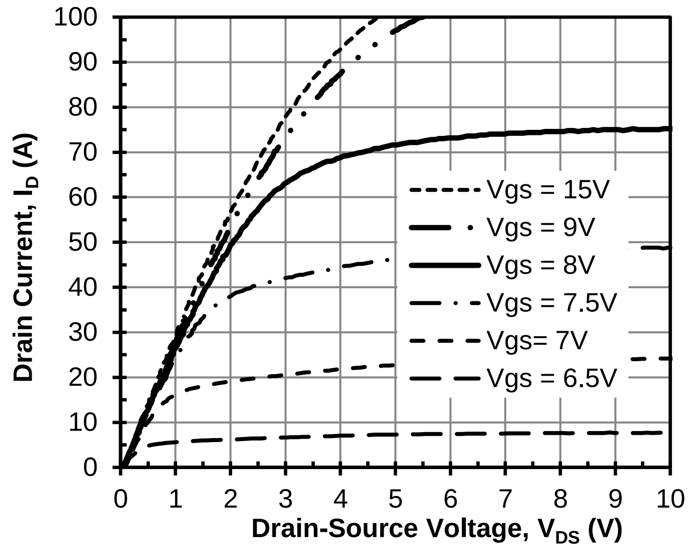


Figure 2 Typical output characteristics at T_j = 25°C, tp < 250 μs

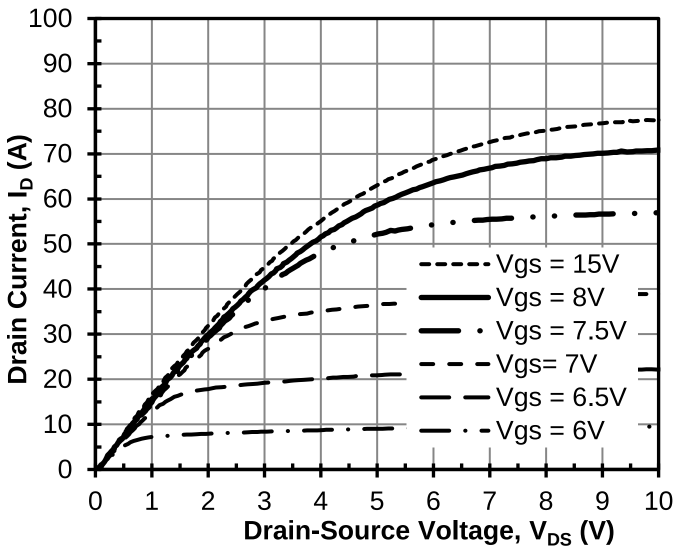


Figure 3 Typical output characteristics at T_j = 150°C, tp < 250 μs

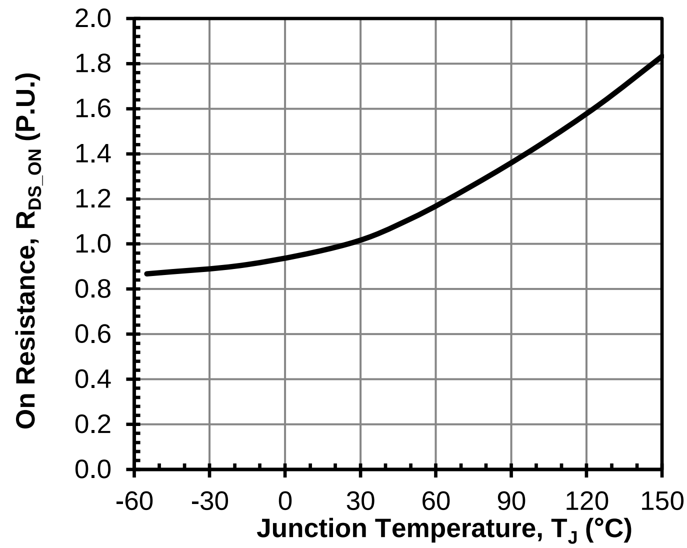


Figure 4 Normalized on-resistance vs. temperature at V_{GS} = 12V and I_D = 25A

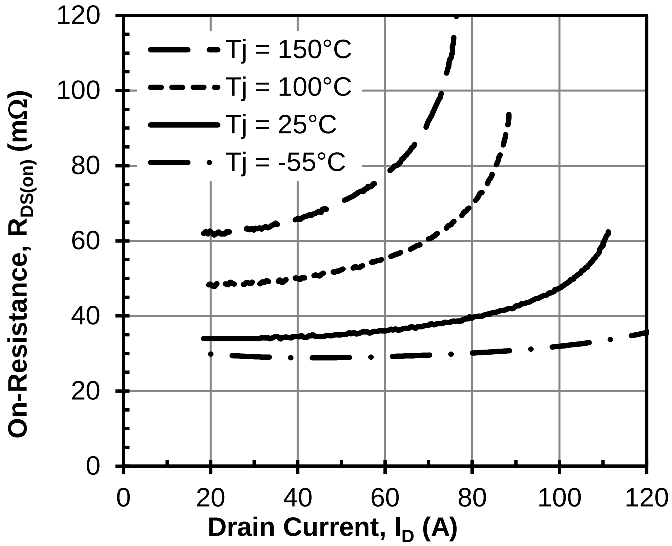


Figure 5 Typical drain-source on-resistance at V_{GS} = 12V

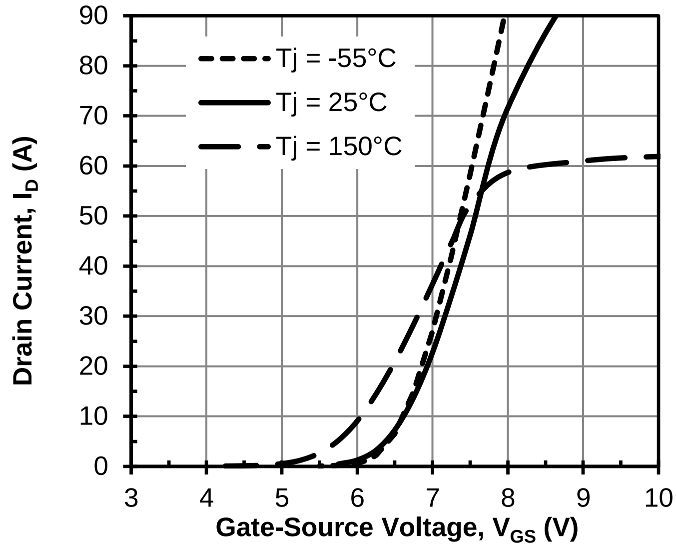


Figure 6 Typical transfer characteristics at V_{DS} = 5V

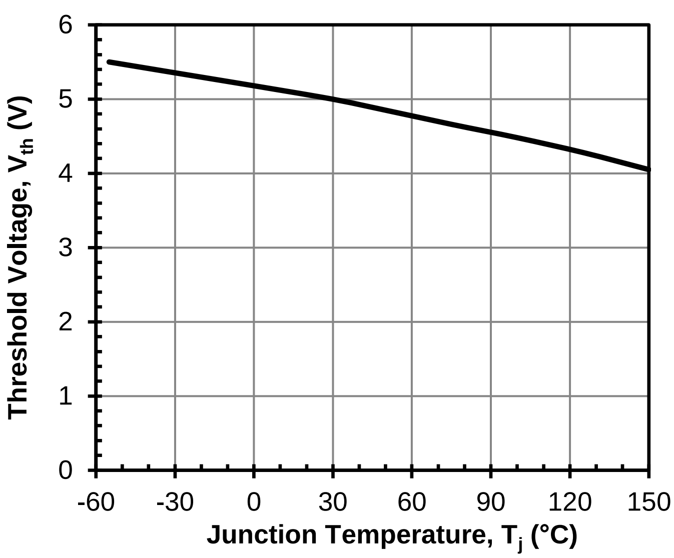


Figure 7 Threshold voltage vs. Tj at V_{DS} = 5V and I_D = 10mA

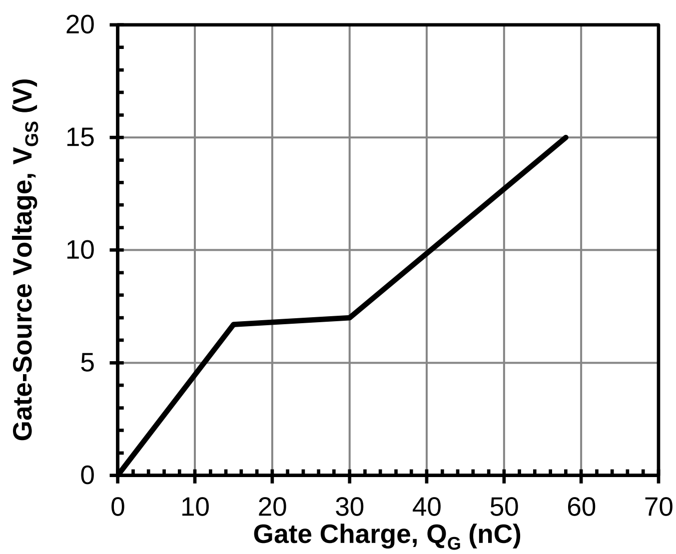


Figure 8 Typical gate charge at V_{DS} = 400V and I_D = 25A

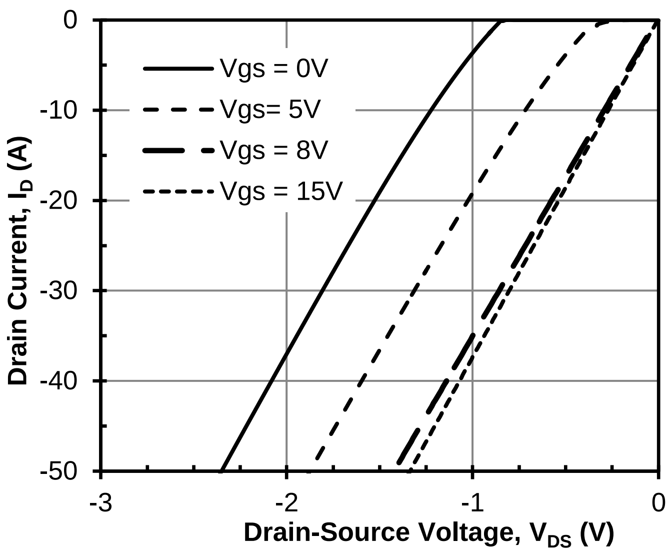


Figure 9 3rd quadrant characteristics at T_J = - 55°C

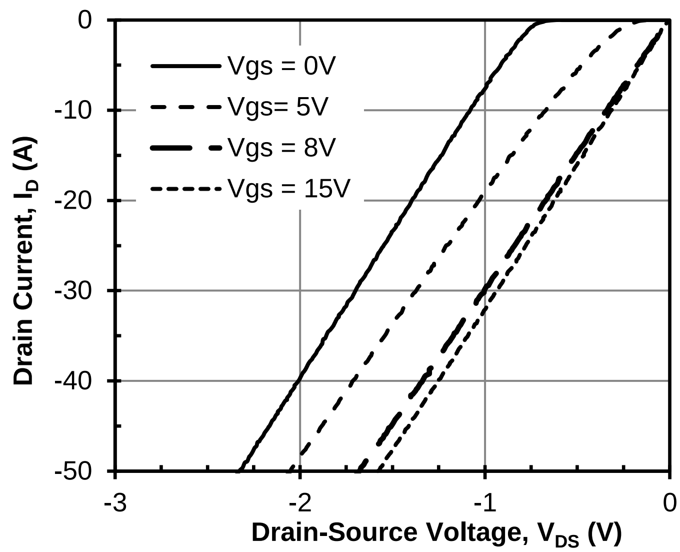


Figure 10 3rd quadrant characteristics at T_J = 25°C

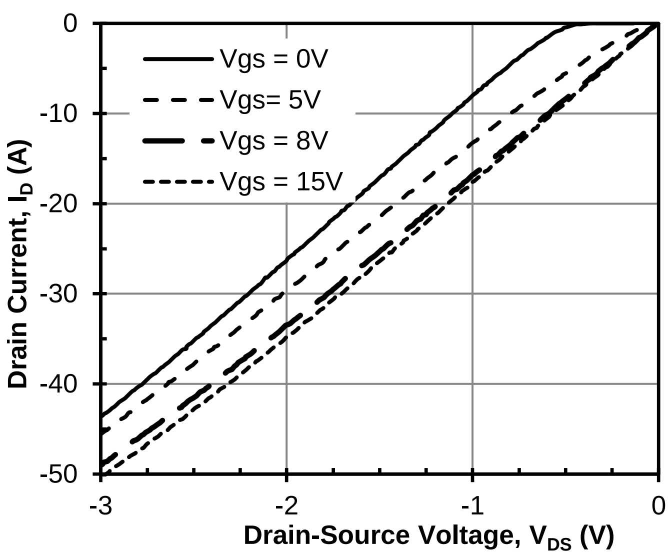


Figure 11 3rd quadrant characteristics at T_J = 150°C

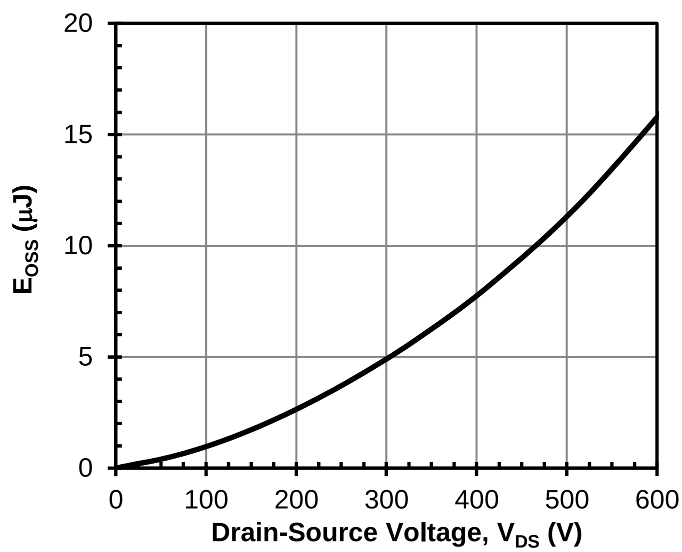


Figure 12 Typical stored energy in C_{OSS} at V_{GS} = 0V

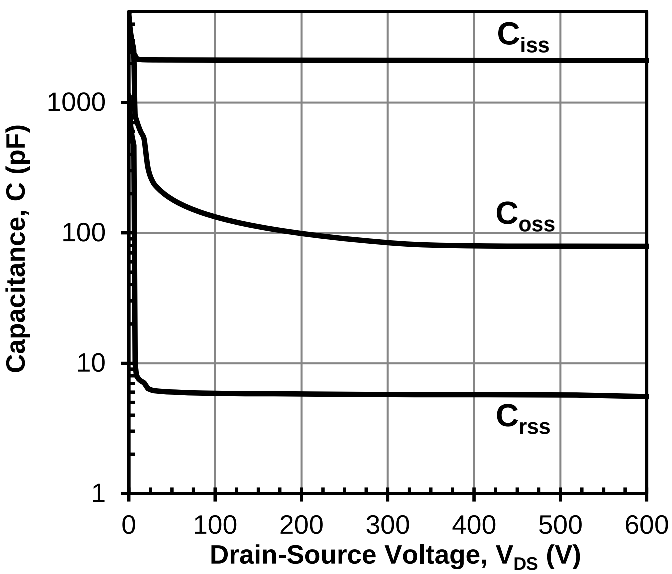


Figure 13 Typical capacitances at 100kHz and V_{GS} = 0V

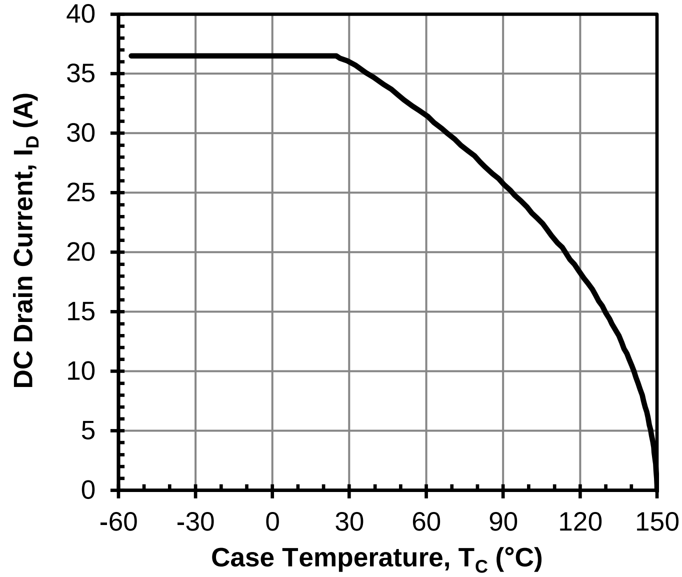


Figure 14 DC drain current derating

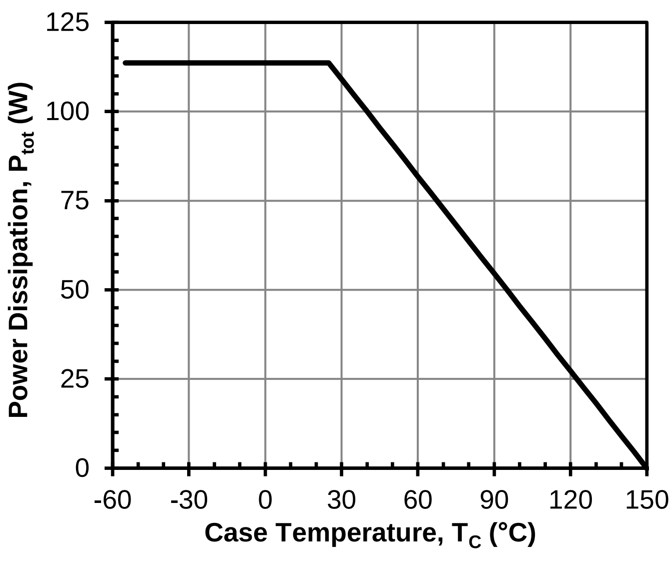


Figure 15 Total power dissipation

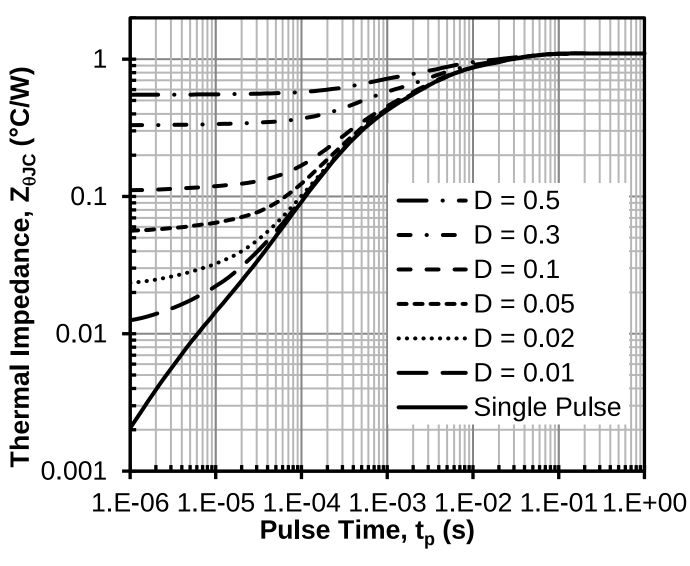


Figure 16 Maximum transient thermal impedance

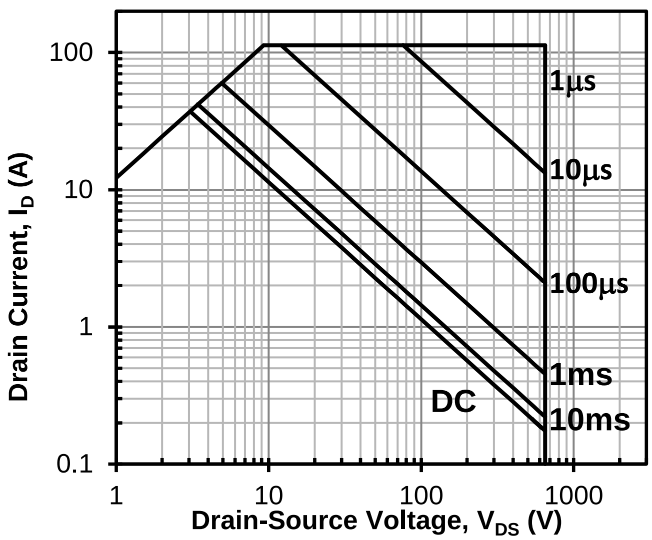


Figure 17 Safe operation area
T_c = 25°C, D = 0, Parameter t_p

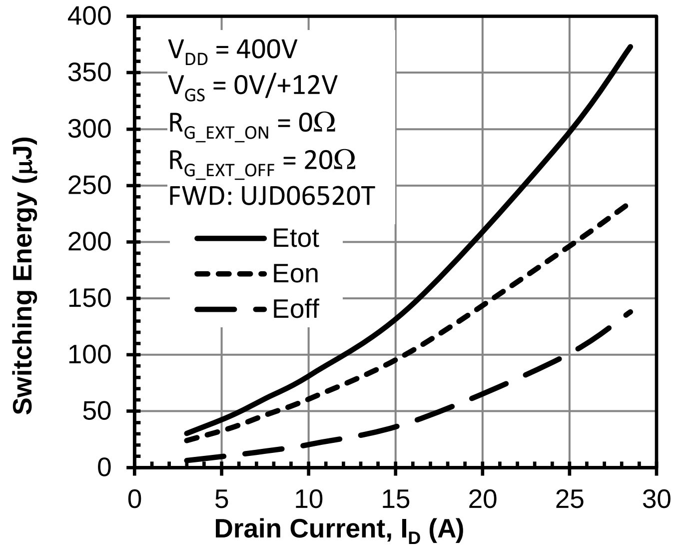


Figure 18 Clamped inductive switching energy vs. drain current at T_J = 25°C

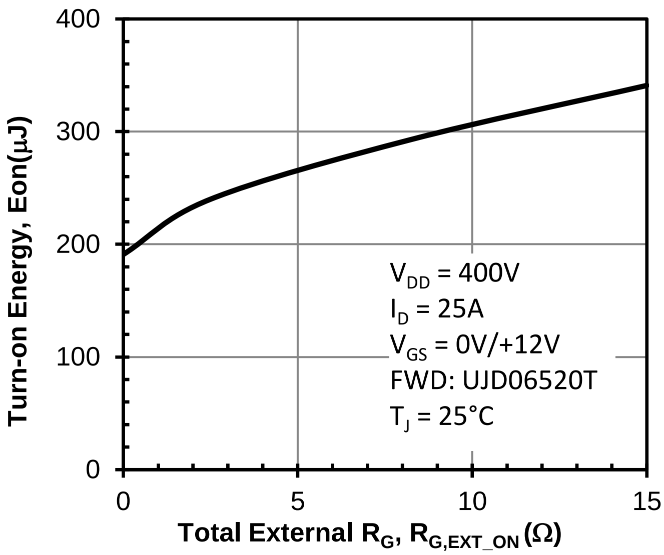


Figure 19 Clamped inductive switching turn-on energy vs. R_{G,EXT_ON}

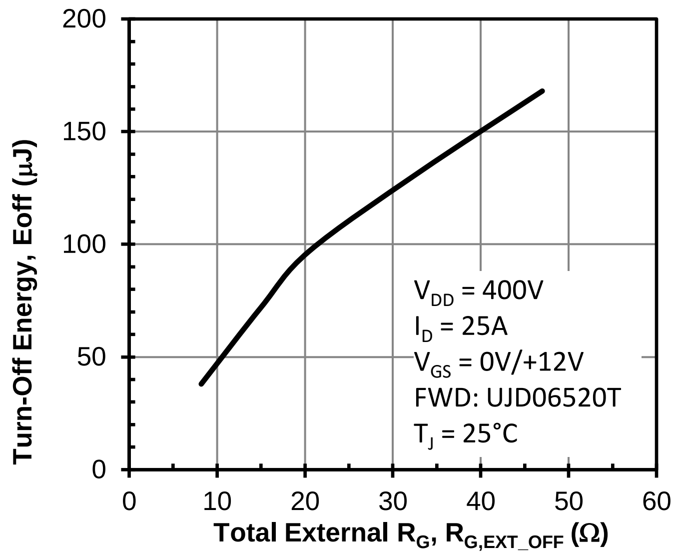


Figure 20 Clamped inductive switching turn-off energy vs. R_{G,EXT_OFF}

Applications Information

SiC cascodes are enhancement-mode power siwtches formed by a high-voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series. The silicon MOSFET serves as the control unit while the SiC JFET provides high voltage blocking in the off state. This combination of devices in a single package provides compatibility with standard gate drivers and offers superior performance in terms of low on-resistance ($R_{DS(on)}$), output capacitance (Coss), gate charge (Qg), and reverse recovery charge (Qrr) leading to low conduction and switching losses. The SiC cascodes also provide excellent reverse conduction capability eliminating the need for an external anti-parallel diode.

Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the high dv/dt and di/dt rates. An external gate resistor is recommended when the cascode is working in the diode mode in order to achieve the optimum reverse recover performance. For more information on cascode operation, see www.unitedsic.com.

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