United Silicon Carbide, Inc.

AEC-Q101 Product Qualification Report

Discrete TO Packaged SiC Diodes

Included Products:

Die	TO-220-2L	TO-247-3L	TO-247-2L
UJ3D06504	UJ3D06504TS	UJ3D06520KSD	UJ3D1210K2
UJ3D06506	UJ3D06506TS	UJ3D06560KSD	UJ3D1220K2
UJ3D06508	UJ3D06508TS	UJ3D1210KS	UJ3D1250K2
UJ3D06510	UJ3D06510TS	UJ3D1210KSD	
UJ3D06530	UJ3D06512TS	UJ3D1220KSD	
UJ3D1202	UJ3D06516TS	UJ3D1250K	
UJ3D1205	UJ3D06520TS		
UJ3D1210	UJ3D06530TS		
UJ3D1220	UJ3D1202TS		
UJ3D1250	UJ3D1205TS		
	UJ3D1210TS		

Scope

This report summarizes the AEC-Q101 qualification results for the UJ3D family of discrete SiC Diodes in Die/Wafers, as well as TO-220-2L, TO-247-3L, and TO-247-2L plastic packages.

The environmental stress tests listed below are performed with pre-stress and post-stress electrical tests. Reviewing the electrical results for new failures and any significant shift in performance satisfies the AEC-Q101 qualification requirements, as well as UnitedSiC Quality requirements.

Reliability Stress Test Summary

Test Name	Test Standard	# Samples x # Lots	Failures
High Temperature Reverse Bias (HTRB)	MIL-STD-750-1 M1038 Method A (1000 Hours) T_J=175°C, V=80% V_{max}	77x12 lots	0/924
High Temperature Reverse Bias (HTRB)	MIL-STD-750-1 M1038 Method A (168 Hours) T_J=175°C, V=80% V_{max}	77x2 lots	0/154
Intermittent Operating Life (IOL)	MIL-STD-750 Method 1037 DT_J ≥125°C, 3000 cycles (5 minutes on/ 5 minutes off)	77x14 lots	0/1078
Intermittent Operating Life (IOL)	MIL-STD-750 Method 1037 DTJ ≥100°C, 6000 cycles (5 minutes on/ 5 minutes off)	77x3 lots	0/231
Highly Accelerated Stress Test (HAST)	JESD22 A-110 (96 Hours) T_A=130°C/85%RH, V=42V	77x12 lots	0/924
Temperature Cycle (TC)	JESD22 A-104 (1000 Cycles)	77x10 lots	0/770
Autoclave (PCT)	JESD22 A-102 121°C/ RH = 100%, 96 hours, 15psig	77x12 lots	0/924

Parametric Verification	Per Datasheet, per product	100% FT x 12 lots	
Physical Dimensions	Per AEC-Q101 Rev D	30x3 packages	0/90

Reliability Evaluation:

The FIT rate data presented below is determined according to JEDEC Standard JESD 85 and is determined from the HTRB Burn-In sample size.

FIT = 1.2685 failures per billion device hours

MTTF = 89993.24 years

From the equations:

$$\lambda_{hours} = \frac{X^2(\alpha,\nu)}{2 \times D \times H \times A_f}$$

$$FIT = \lambda_{hours} \times 10^9$$

$$MTTF_{hours} = {}^{1}/_{\lambda_{hours}}$$

And

$$A_f = e^{\frac{E_a}{k}\left(\frac{1}{T_{use}} - \frac{1}{T_{test}}\right)}$$

Where:

X^2 = Chi-Squared probability function for a given Confidence Level (α) and Degree of Freedom ($\nu = 2r+2$, where r = the number of failures in the Test Population),

D = Number of Devices in the Test Population,

H = Test Hours per Device,

A_f = Acceleration Factor from the Arrhenius equation,

E_a = Activation Energy (eV),

T_{use} = standardized Use Temperature,

T_{test} = Temperature of Stress Test,

and

k = Boltzmann's Constant.

In our calculations, we used our HTRB Burn-In data:

D = 924 devices for HTRB at 1000H and 154 devices at 168H

H = 1000 hours and 168 hours in different HTRB sample sets

$1 - \alpha$ = 0.6 (60% Confidence Level)

r = 0 Failures

E_a = 0.7 eV

T_{use} = 55 °C or 328 K

T_{test} = 175 °C or 448 K