United Silicon Carbide, Inc.

AEC-Q101 Product Qualification Report

Discrete Surface Mount Devices

Included Products:

D2PAK-3L

UF3C065080B3

UF3C065040B3

UF3C065030B3

UJ3C065080B3

UJ3C065030B3

This report summarizes the AEC-Q101 qualification results for the UF3C and UJ3C family of Discrete SiC Cascodes in D2Pak-3L plastic packages.

The environmental stress tests listed below are performed with pre-stress and post-stress electrical tests. Reviewing the electrical results for new failures and any significant shift performance satisfies the AEC-Q101 qualification requirements, as well as UnitedSiC's Quality requirements.

Reliability Stress Test Summary

Test Name	Test Standard	# Samples x # Lots	Failures
High Temperature Reverse Bias (HTRB)	MIL-STD-750-1 M1038 Method A (1000 Hours) T_J=175°C, V=80% V_{max}	77x3 lots	0/231
High Temperature Gate Bias (HTGB)	JESD22 A-108 (1000 Hours) T_J=175°C, V=100% V_{max} (+25V), bias in on direction	77x3 lots	0/231
MSL1 Preconditioning	JEDEC Standard 22-A113D (168 Hours) T_A=85°C/85%RH	77x10 lots & 30x1lot	0/800
Highly Accelerated Stress Test (HAST)†	JESD22 A-110 (96 Hours) T_A=130°C/85%RH	77x3 lots	0/231
Intermittent Operating Life (IOL)†	MIL-STD-750 Method 1037 DT_J ≥125°C, 3000 cycles (5 minutes on/ 5 minutes off)	77x1 lots	0/77
Temperature Cycle (TC)†	JESD22 A-104 (1000 Cycles)	77x3 lots	0/231
Autoclave (PCT)†	JESD22 A-102 121°C/ RH = 100%, 96 hours, 15psig	77x3 lots	0/231
Resistance to Solder Heat (RSH)†	JESD22 A-111(SMD)	30x1 lot	0/30

Parametric Verification	Per Datasheet	100% FT x 3 lots	
Physical Dimensions	Per AEC-Q101 Rev D	30x1 packages	0/30
ESD – Charged Device Model	AEC-Q101-005 Field Induced Charged-Device Model, 3 positive and 3 negative pulses applied to All Pins	30x1 lots	0/30
ESD – Human Body Model	AEC-Q101-001 Human Body Model: R=1500 ohm, C=100 pf, 3 positive and 3 negative pulses applied to All Pins	30x1 lots	0/30
Bondline Thickness	Per Assembly Spec	10x3 lots	0/30
Die Shear	Per Assembly Spec	10x3 lots	0/30
Die Attach Voids	Per Assembly Spec	10x3 lots	0/30
Wire Pull	Per Assembly Spec	10x3 lots	0/30
Wedge Shear	Per Assembly Spec	10x3 lots	0/30
CSAM	Per Assembly Spec	60x3 lots	0/180
Lead Integrity Test	Per AEC-Q101 Rev D	30x1 lots	0/30
Solderability Test	Per AEC-Q101 Rev D	10x1 lots	0/10

†:HAST, PCT, TC, IOL, and RSH samples were subjected to MSL1 Pre-Conditioning before their tests.

Reliability Evaluation:

The FIT rate data presented below is determined according to JEDEC Standard JESD 85 and is determined from the HTRB and HTGB Burn-In sample size.

FIT = 2.608009 failures per billion device hours

MTTF = 43771 years

From the equations:

$$\lambda_{hours} = \frac{X^2(\alpha, \nu)}{2 \times D \times H \times A_f}$$

$$FIT = \lambda_{hours} \times 10^9$$

$$MTTF_{hours} = {}^{1}/_{\lambda_{hours}}$$

And

$$A_f = e^{\frac{E_a}{k}\left(\frac{1}{T_{use}} - \frac{1}{T_{test}}\right)}$$

Where:

X^2 = Chi-Squared probability function for a given Confidence Level (α) and Degree of Freedom ($\nu = 2r+2$, where r = the number of failures in the Test Population),

D = Number of Devices in the Test Population,

H = Test Hours per Device,

A_f = Acceleration Factor from the Arrhenius equation,

E_a = Activation Energy (eV),

T_{use} = standardized Use Temperature,

T_{test} = Temperature of Stress Test,

and

k = Boltzmann's Constant.

In our calculations, we used our HTGB and HTRB Burn-In data:

D = 231 devices for HTGB and 231 for HTRB,

H = 1000 hours for HTGB and 1000 hours of HTRB,

$1 - \alpha$ = 0.6 (60% Confidence Level)

r = 0 Failures

E_a = 0.7 eV

T_{use} = 55 °C or 328 K

T_{test} = 175 °C or 448 K