United Silicon Carbide, Inc.

AEC-Q101 Product Qualification Report

Discrete TO-247 Stacked Cascode Devices

Included Products:

TO-247-4L	TO-247-3L
UF3SC065007K4S	UF3SC120016K3S
UF3SC120009K4S	
UF3SC120016K4S	

This report summarizes the AEC-Q101 qualification results for the 650V and 1200V UF3SC Discrete SiC Cascodes in TO-247-3L and TO-247-4L plastic packages.

The environmental stress tests listed below are performed with pre-stress and post-stress electrical tests. Reviewing the electrical results for new failures and any significant shift in performance satisfies the qualification requirements.

Reliability Stress Test Summary

Test Name	Test Standard	# Samples x # Lots	Failures
High Temperature Reverse Bias (HTRB)	MIL-STD-750-1 M1038 Method A (1000 Hours) T_J=175°C, V=80% V_{max}	26x3 lots 650V, 33x1 + 77x3 lots 1200V	0/342
High Temperature Gate Bias (HTGB)	JESD22 A-108 (1000 Hours) T_J=175°C, V=100% V_{max} (+20V), bias in one direction	26x3 lots 650V, 33x1 + 77x3 lots 1200V	0/342
High Humidity, High Temperature Reverse Bias (H3TRB)	JESD22-A101C (1000 Hours) T_A=85°C, 85% RH, V_{GS}=0V, V_{DS}=100V	26x3 lots 650V, 33x1 + 77x3 lots 1200V	0/342
Temperature Cycle (TC)	JESD22 A-104 (1000 Cycles)	26x3 lots 650V, 33x1 + 77x3 lots 1200V	0/342
Autoclave (PCT)	JESD22 A-102 121°C/ RH = 100%, 96 hours, 15psig	26x3 lots 650V, 33x1 + 77x3 lots 1200V	0/342
Intermittent Operating Life	MIL-STD-750 Method 1037 DTJ ≥125°C, 3000 cycles (5 minutes on/ 5 minutes off)	77x3 lots 1200V	0/231
Parametric Verification	Per Datasheet	100% FT x 7 lots	

Physical Dimensions	Per AEC-Q101 Rev D	30x1 packages	0/30
Bondline Thickness	Per Assembly Spec	10x3 lots	0/30
Die Shear	Per Assembly Spec	10x3 lots	0/30
Die Attach Voids	Per Assembly Spec	10x3 lots	0/30
Wire Pull	Per Assembly Spec	10x3 lots	0/30
Wedge Shear	Per Assembly Spec	10x3 lots	0/30
CSAM	Per Assembly Spec	60x3 lots	0/180
Lead Integrity Test	Per AEC-Q101 Rev D	30x1 lots	0/30
Solderability Test	Per AEC-Q101 Rev D	10x1 lots	0/10

ESD Testing:

UnitedSiC FETs have integrated ESD protection. The ESD protection will vary with the chip size. All products will meet a minimum rating of C3 (>1000V) for the Charged Device Model, and H2 (>2000V and <4000V) for the Human Body Model.

Reliability Evaluation:

The FIT rate data presented below is determined according to JEDEC Standard JESD 85 and is determined from the HTRB and HTGB Burn-In sample size.

FIT = 1.76155014 failures per billion device hours

MTTF = 64803.86 years

From the equations:

$$\lambda_{hours} = \frac{X^2(\alpha, \nu)}{2 \times D \times H \times A_f}$$

$$FIT = \lambda_{hours} \times 10^9$$

$$MTTF_{hours} = {}^{1}/_{\lambda_{hours}}$$

And

$$A_f = e^{\frac{E_a}{k}\left(\frac{1}{T_{use}} - \frac{1}{T_{test}}\right)}$$

Where:

X^2 = Chi-Squared probability function for a given Confidence Level (α) and Degree of Freedom ($\nu = 2r+2$, where r = the number of failures in the Test Population),

D = Number of Devices in the Test Population,

H = Test Hours per Device,

A_f = Acceleration Factor from the Arrhenius equation,

E_a = Activation Energy (eV),

T_{use} = standardized Use Temperature,

T_{test} = Temperature of Stress Test,

and

k = Boltzmann's Constant.

In our calculations, we used our HTGB and HTRB Burn-In data:

D = 342 devices for HTGB and 342 for HTRB,

H = 1000 hours for HTGB and 1000 hours of HTRB,

$1 - \alpha$ = 0.6 (60% Confidence Level)

r = 0 Failures

E_a = 0.7 eV

T_{use} = 55 °C or 328 K

T_{test} = 175 °C or 448 K