$$L \geq \frac{D(1-D)V_{out}V_{in\_min}}{0.2 * \sqrt{2}P_{out}f_{sw}} \quad (1)$$

For this prototype the inductor is fabricated manually with 2 stacks of C055438A2 MPP cores. The winding consists of 25 turns of 2-strand AWG-14 magnet wires. The inductance is 150 µH at full load and 350 µH at no load. The inductor DC resistance is 14 mΩ.

The output capacitance is determined based on two constraints, load hold-up time and output voltage ripple regulation. In this design, the hold-up time is set to be one AC line cycle and the output voltage peak to peak ripple is set to be 10 V.

$$C_{out} \geq \frac{2P_o t_{holdup}}{V_o^2 - V_{o\_min}^2};\ C_{out} \geq \frac{P_o}{2V_o \pi f_{line} V_{ripple}} \quad (2)$$

To meet both criteria, two 560 µF, 500 V aluminum electrolytic capacitors are used in parallel for this prototype.

The +12/-5 V gate drive is designed with isolated DCDC power supply module, RP-1212D, and -5 V linear voltage regulator, LT1175CS8-5#PBF. It is important to use isolated DC-DC power supply module with very small isolation capacitance to reduce common mode noise from the switch node fast dv/dt transients.

The zero-crossing current spike is an inherent challenge of totem-pole PFC. This phenomenon will increase THD and decrease power factor. It is caused by the sudden discharge of the parasitic output capacitance of Q3 (from positive to negative cycle zero-crossing) or Q4 (from negative to positive cycle zero-crossing) when the corresponding fast leg active switch turns on. For example, during a zero-crossing from negative to positive cycle, Q2 becomes the active switch in the fast leg. Since input voltage is nearly zero, in order to output 400 V the duty ratio of Q2 is almost 100% while Q4 was blocking 400 V during the negative half cycle. Therefore, when Q2 turns on, the charge stored in the parasitic output capacitance of Q4 will incur a positive current spike on the input inductor. To gradually discharge the parasitic output capacitance of the slow leg Si MOSFET multiple gate pulses with small duty ratio are applied after a blanking window at zero-crossing. Experimental results show a very good mitigation of zero-crossing current spikes with this method.

4 Experiment Result

Figure 2 is the prototype of the 1.5 kW hard switched CCM totem-pole bridgeless PFC. No input filter is used for the measurement. Both AC input and DC output are floating. All voltage waveforms are obtained through differential probes. The input power, PF and THD is measured by a Tektronix PA1000 single phase power analyzer. The output power is measured by a Tektronix PA1000 single phase power analyzer.

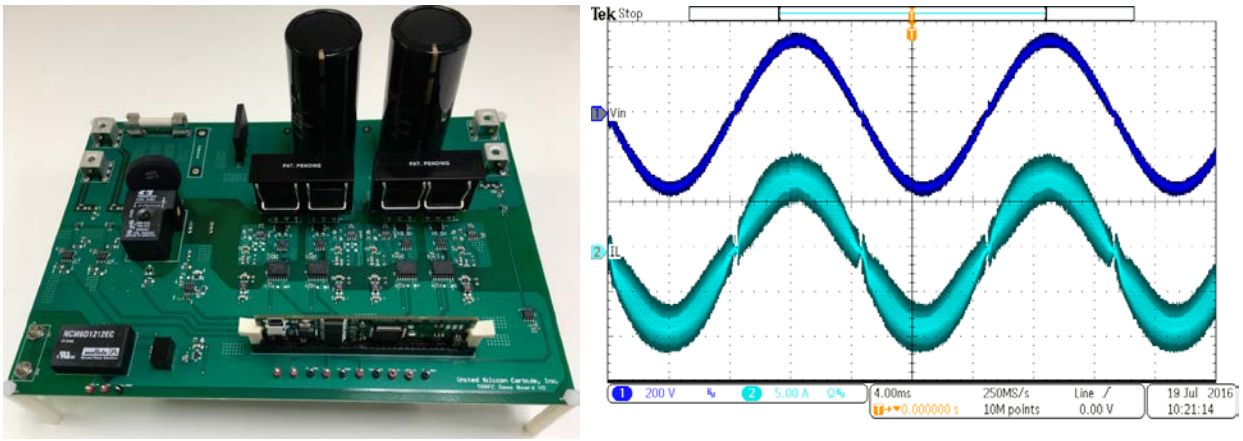

Figure 2. 1.5 kW hard switched CCM totem-pole PFC prototype (left) and input voltage, inductor current at 230 VAC, 1.3 kW load (right).

Figure 3 shows the efficiency curve measured at 230 VAC with 0 Ω turn-on gate resistor and 10 Ω turn-off gate resistor for the UJC06505K. 99.4% peak efficiency and 3.77% THD is achieved with 230 V AC input at 100 kHz switching frequency.

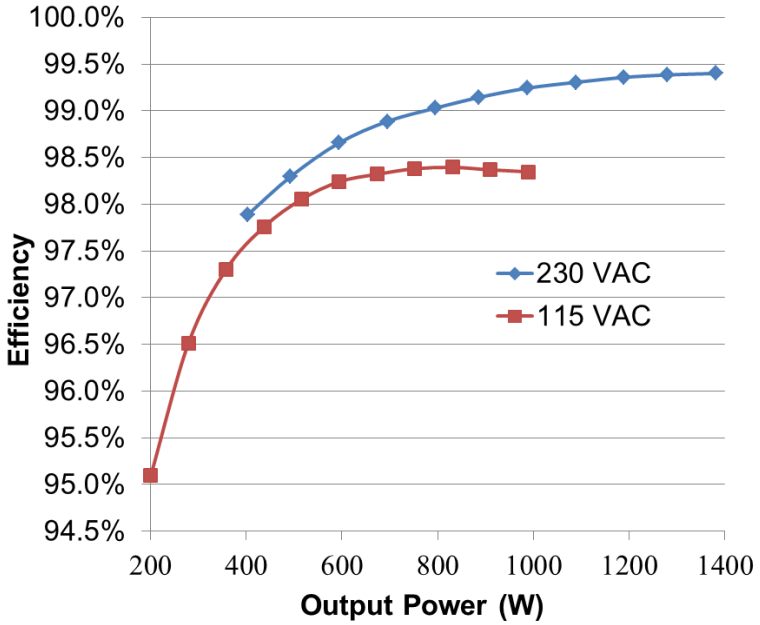

Figure 3. Efficiency at 230 VAC input

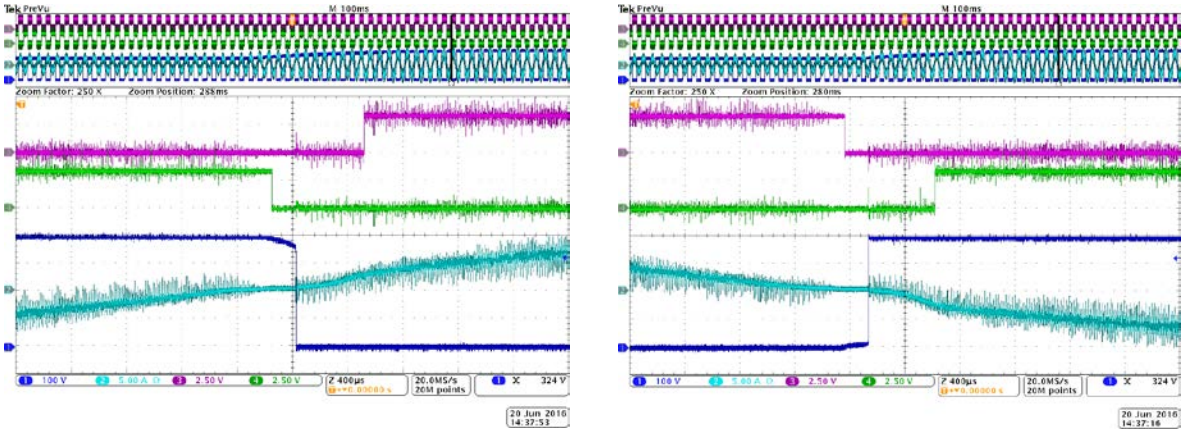

Figure 4. Inductor current (light blue CH2) at zero crossing, from negative to positive (left), from positive to negative (right). (CH1: VN potential to DC output ground; CH3: DSP gate signal of Q4; CH4: DSP gate signal of Q3)

As shown in Figure 4, with a blank window and low duty ratio gate pulses of the active device in the fast switching leg, current spikes near zero-crossing is greatly reduced.

5 Conclusion

A hard switched CCM totem-pole PFC is realized using the UnitedSiC UJC06505K 650 V SiC cascodes. Neglecting control and gate drive power, 99.4% peak efficiency is achieved at 100 kHz switching frequency in the fast switching leg with 230 V high line condition. The low RDS(on), low Qrr and fast switching capability make 650 V SiC cascodes

ideal for full-bridge and half-bridge hard switching applications. Figure 2 demonstrates that the input inductor current follows the input AC voltage very well. Figure 4 illustrates that current spike near zero-crossing of input AC voltage is substantially alleviated by a blank window and multiple gate pulses of the active switch in the fast leg with small duty ratio.

References

[1] Q. Li, M. A. E. Andersen and O. C. Thomsen, "Conduction losses and common mode EMI analysis on bridgeless power factor correction," *2009 International Conference on Power Electronics and Drive Systems (PEDS)*, Taipei, 2009, pp. 1255-1260.